

DJ2 Montevina UMA Schematics Document

uFCPGA Mobile Penryn

Intel GM45+ICH9M

2010-06-02

REV : X00

DY : Nopop Component
HDMI : Pop for HDMI
GIGA : Pop for GIGA LAN
10/100 : Pop for 10/100 LAN

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

DJ2 Montevina UMA

Rev

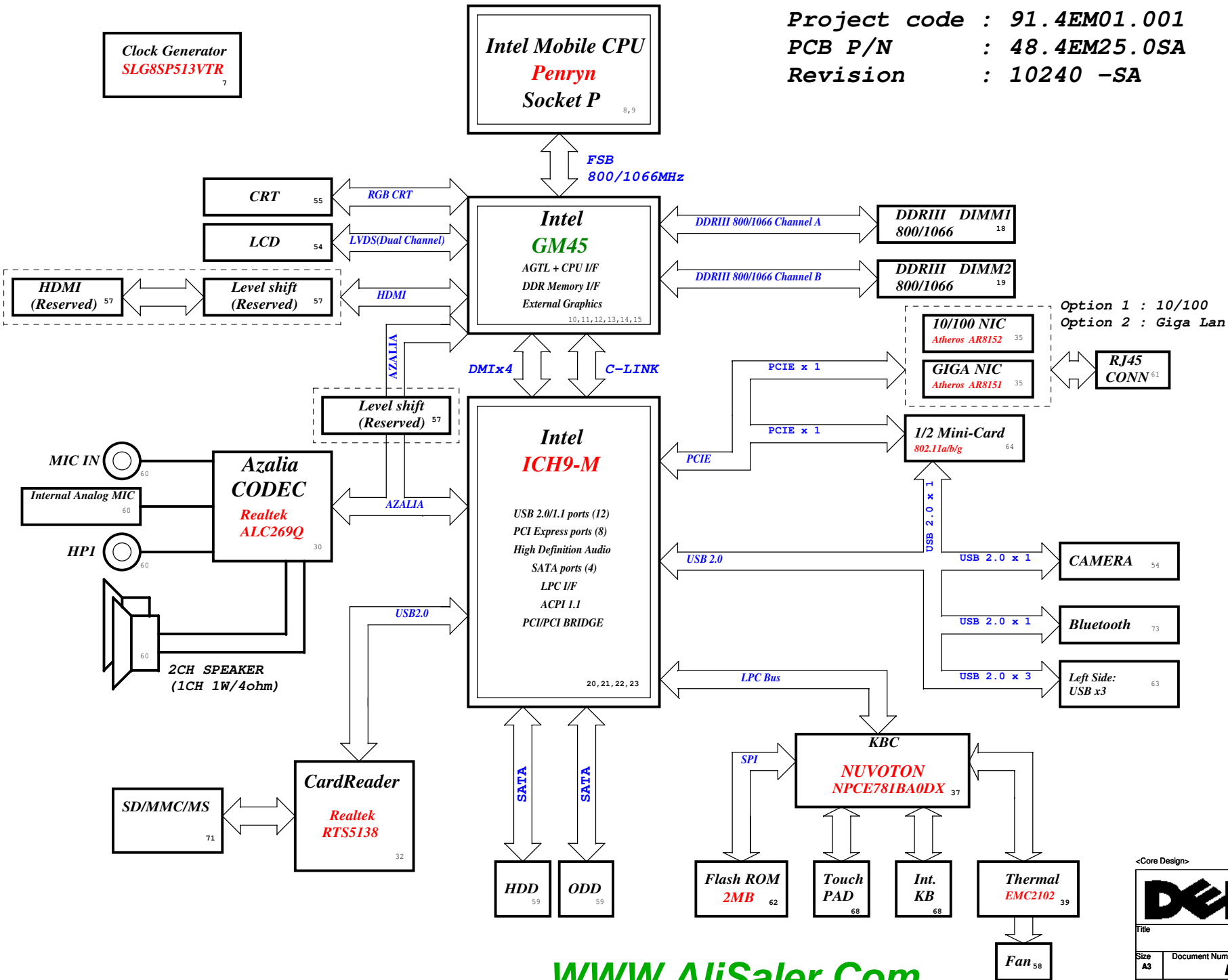
X00

Date: Wednesday, June 02, 2010

Sheet 1 of 88

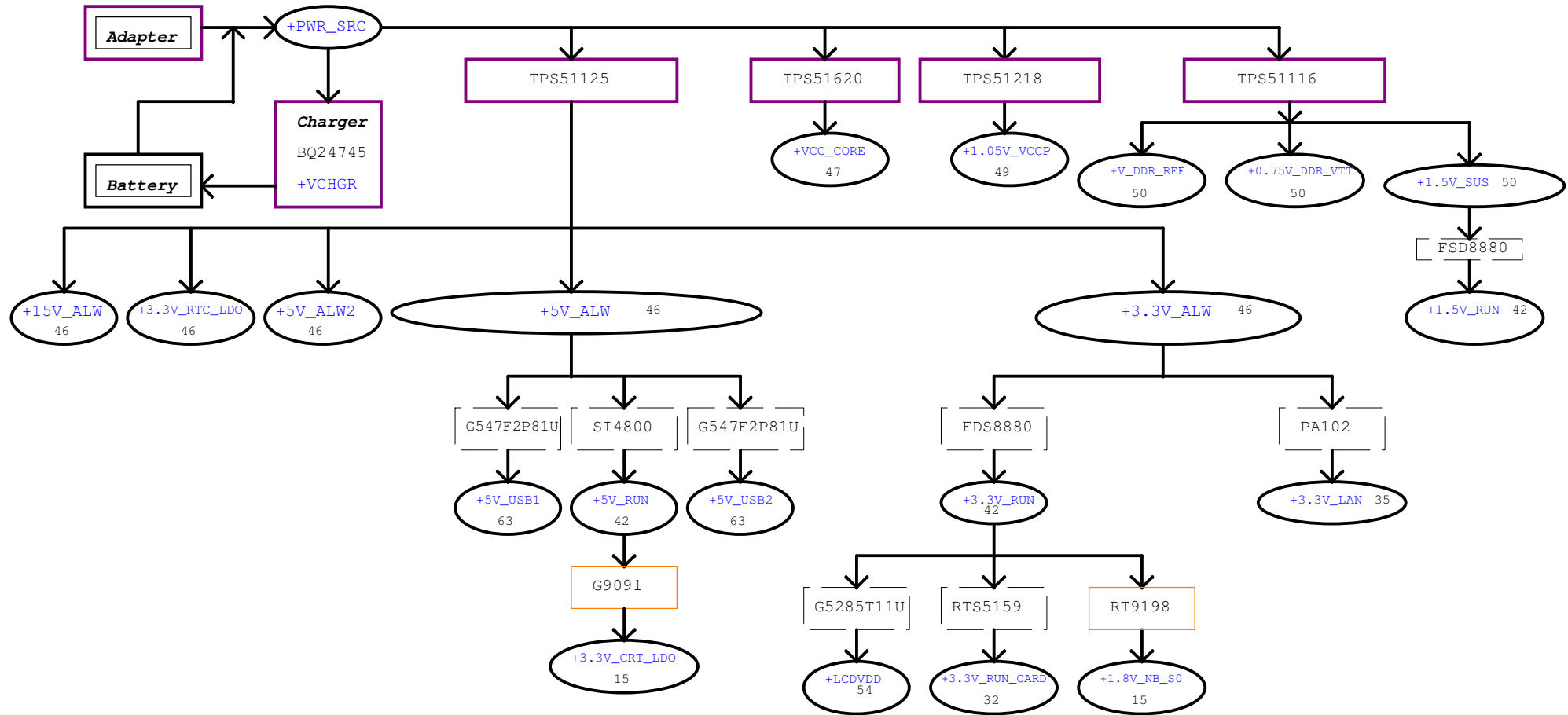
DJ2 Montevina UMA Block Diagram

Project code : 91.4EM01.001
PCB P/N : 48.4EM25.0SA
Revision : 10240 -SA



CPU DC/DC TPS51620	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VCCP
SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
MAXIM CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1: Top	
L2: GND	
L3: Signal	
L4: Signal	
L5: VCC	
L6: Bottom	

DJ1 Montevina UMA Power Block Diagram



Power Shape

Regulator

LDO

Switch

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

Size

Document Number

Rev

A3

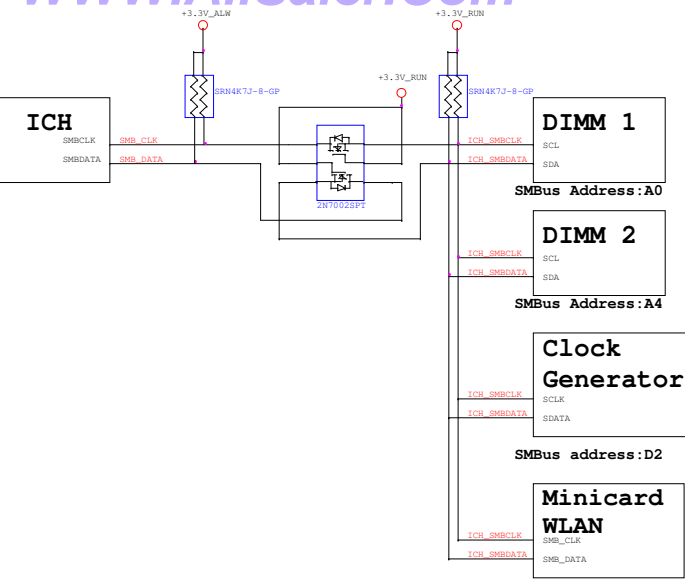
DJ2 Montevina UMA

X00

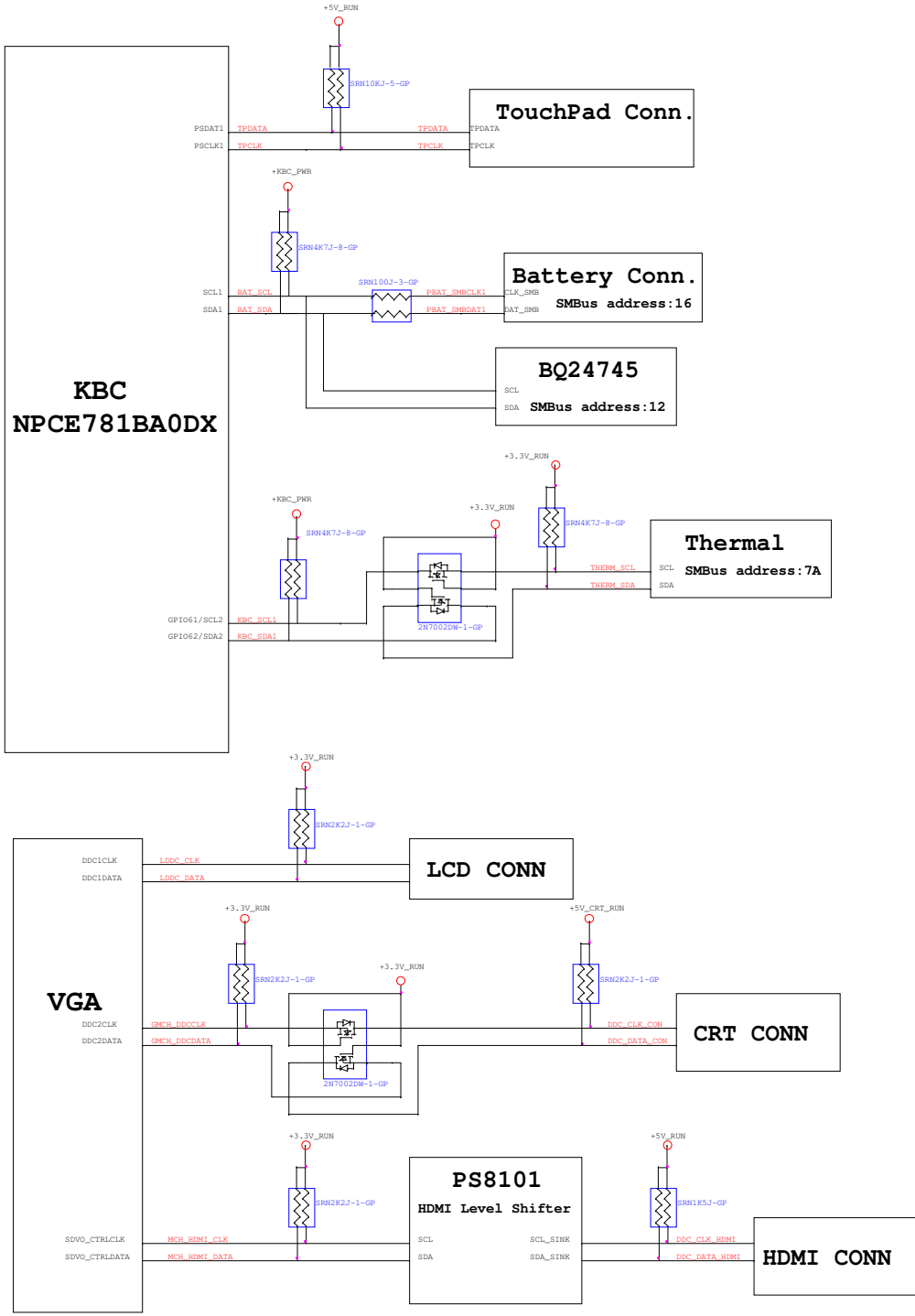
Date: Friday, May 28, 2010

Sheet 3 of 88

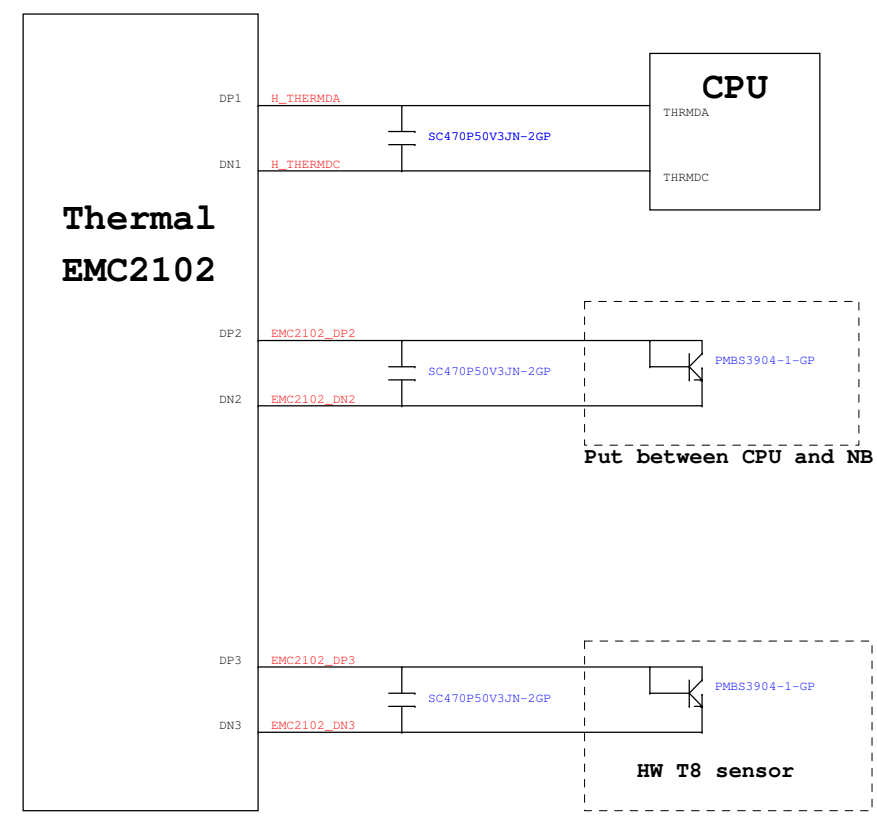
ICH SMBus Block Diagram



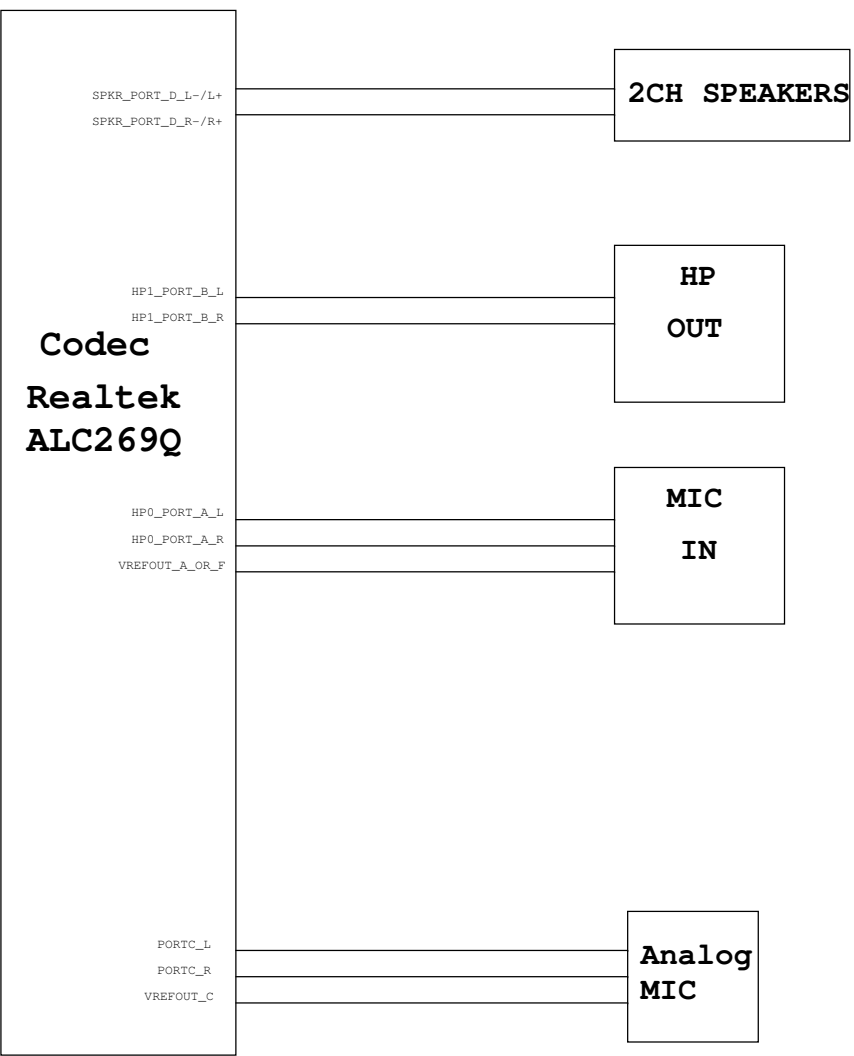
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance / PCI Express* Port Config 1 bit 1 (Port 1-4), Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Config Registers: Offset 224h). This signal has a weak internal pull-down.
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4), Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Config Registers: Offset 224h).
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6), Rising Edge of PWROK	This signal has a weak internal pull-up. Sets bit 2 of RPC.PC2 (Chipset Config Registers: Offset 0224h) when sampled low.
GPIO20	Reserved, Rising Edge of PWROK	This signal has a weak internal pull-down. NOTE: This signal should not be pulled high
GNT1# / GPIO51	ESI Strap (Server Only), Rising Edge of PWROK.	Tying this strap low configures DMI for ESIncompatible operation. This signal has a weak internal pull-up. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3# / GPIO55	Top-Block Swap override. Rising Edge of PWROK.	Sampled low: this indicates that the system is strapped to the "top-block swap" mode (IntelR ICH9 inverts A16 for all cycles targeting BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Config Registers: Offset 3414h: bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#	Boot BIOS Destination Selection 1, Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SPI_CS1# / GPIO58	Boot BIOS Destination Selection 0, Rising Edge of CLPWROK	Controllable via Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h: bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. <div> <div>Bit11 (GNT0#)</div> <div>Bit 10 (SPI_CS1#)</div> <div>Boot BIOS Destination</div> <div> <div>0</div> <div>1</div> <div>1</div> <div>0</div> </div> <div> <div>SPI</div> <div>PCI</div> <div>LPC</div> <div>Reserved</div> </div> </div>
SATALED#	PCI Express Lane Reversal (Lanes 1-4). Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0: Offset D8)
SPKR	No Reboot, Rising Edge of PWROK.	Sampled high: this indicates that the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h: bit 5).
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33 / HDA_DOCK_EN#	Flash Descriptor Security Override Strap. Rising Edge of PWROK. (Mobile Only)	Sampled low: the Flash Descriptor Security will be overridden. Sampled high: the security measures will be in effect. This strap should only be enabled in manufacturing environments.
GPIO49	DMI Termination Voltage. Rising Edge of CLPWROK.	The signal is required to be high for mobile applications.
SPI_MOSI (Mobile Only)	Integrated TPM Enable. Rising Edge of CLPWROK.	Sampled low: the Integrated TPM will be disabled. Sampled high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enabled. NOTE: This signal is required to be floating or pulled low for desktop applications.

ICH9 Integrated pull-up and pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRS1PVR/GPIO16	PULL-DOWN 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT0#, GNT[3:1]# / GPIO[55, 53, 51]	PULL-UP 20K
GPIO20	PULL-DOWN 20K
GPIO49	PULL-UP 20K
LAD[3:0]# / FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ0	PULL-UP 20K
LDRQ1 / GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1# / GPIO58 (Desktop Only) / CLGPIO6 (Digital Office Only)	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH[3:0]	PULL-UP 20K
TP3	PULL-UP 20K
USB[11:0] [P,N]	PULL-DOWN 15K

PCIE Routing

LANE1	
LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB Pair	Device
0	USB0
1	RESERVED
2	USB2
3	USB3
4	BLUETOOTH
5	RESERVED
6	WLAN
7	RESERVED
8	RESERVED
9	RESERVED
10	Card Reader
11	CAMERA

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

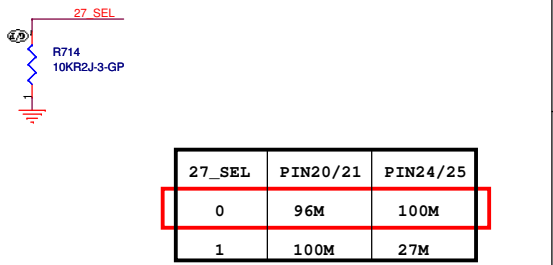
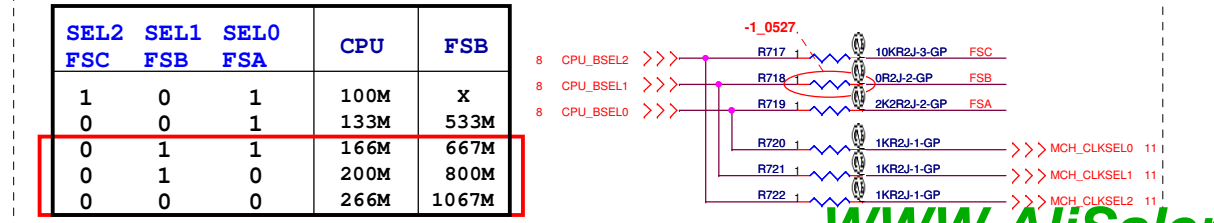
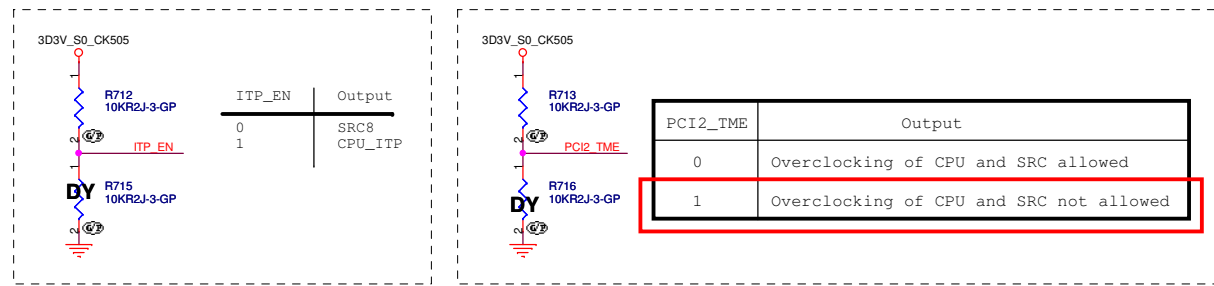
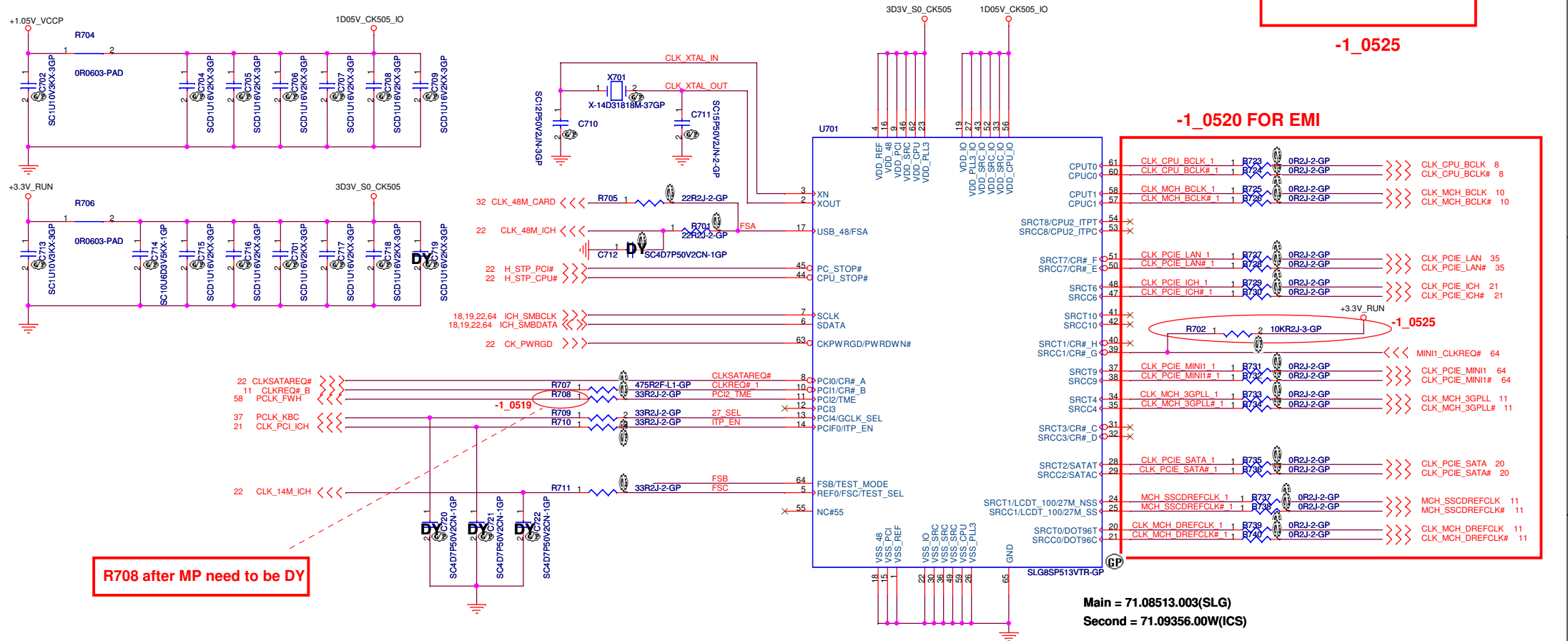
Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Others = Reserved
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	ITPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2). 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management engine crypto strap	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 etc. 1 = Normal operation (default): Lane Numbered in Order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disable (Default)
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) 1 = Disable (Default)
CFG13	XOR	0 = XOR mode enabled (Note 3) 1 = Disable (Default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIE	0 = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) 1 = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA (Note4)	SDVO Present	0 = No SDVO/HDMI/DP interface disabled (default) 1 = SDVO/HDMI/DP interface enabled
LDDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled
DDPC_CTRLDATA (Note4)	Digital Display Present	0 = Digital display (HDMI/DP) device absent (default) 1 = Digital display (HDMI/DP) Device Present
CFG4:3 CFG8 CFG11 CFG14 CFG15 CFG17 CFG18	Reserved	

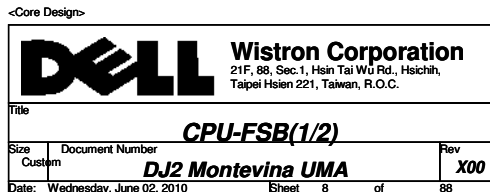
NOTE:

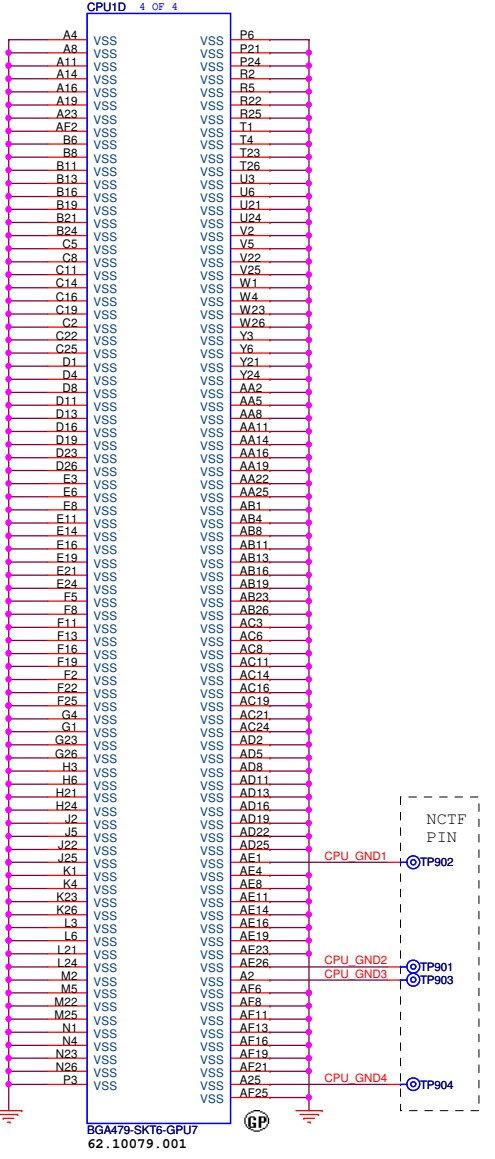
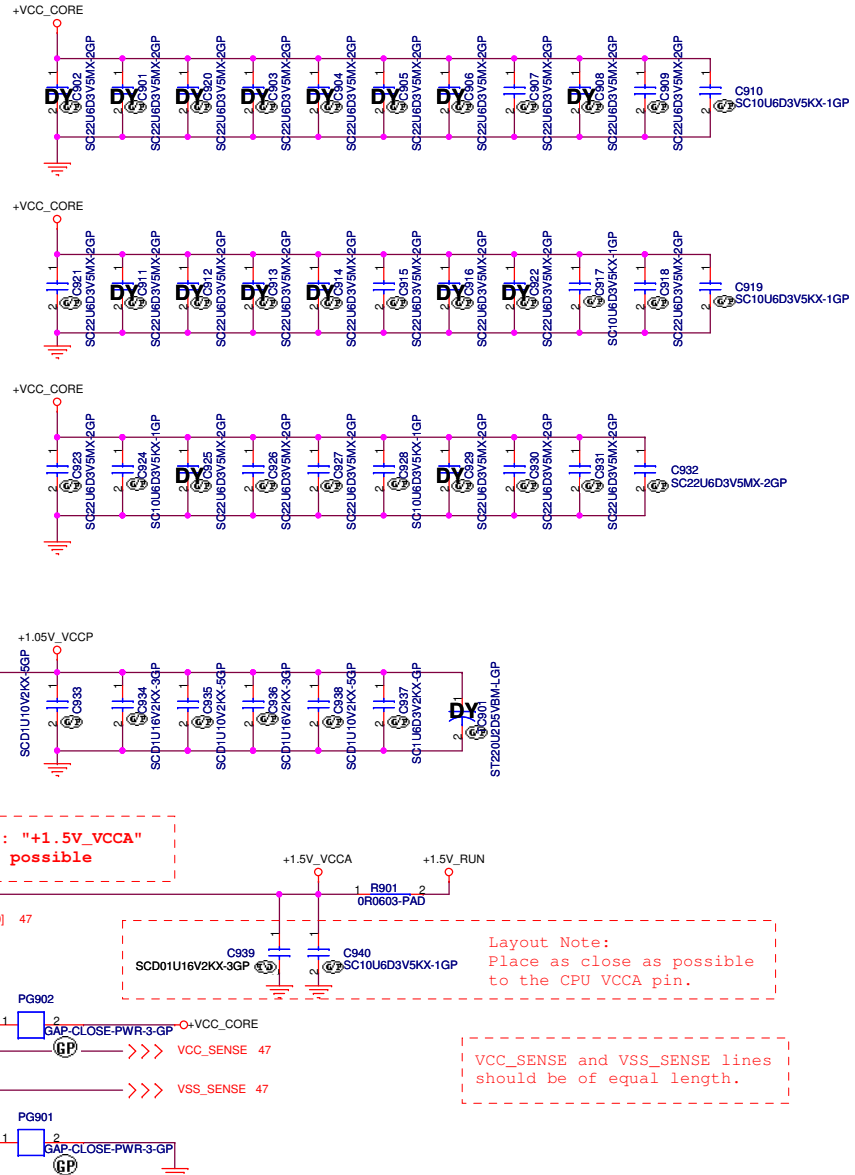
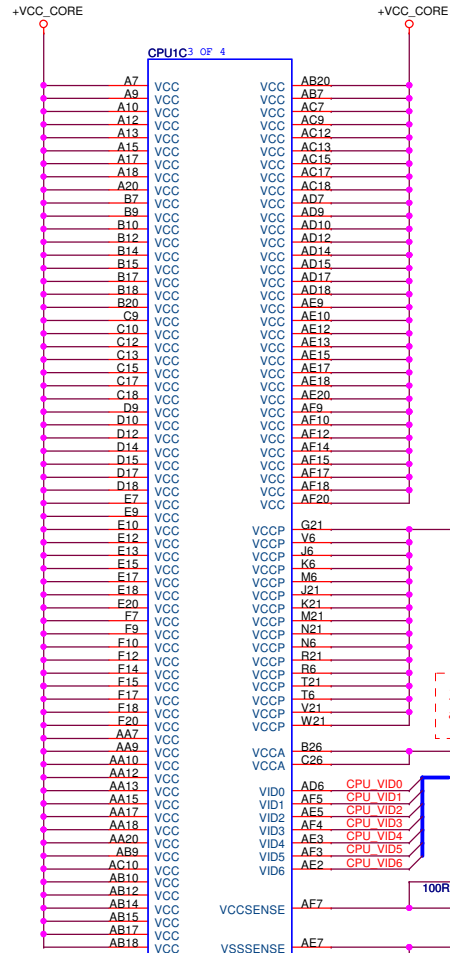
- All strap signals are sampled with respect to the leading edge of the GMCH Power OK (PWROK) signal.
- iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
- Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.
- DDPC_CTRL_DATA & SDVO_CTRL_DATA straps should both be high to enable Display Port.

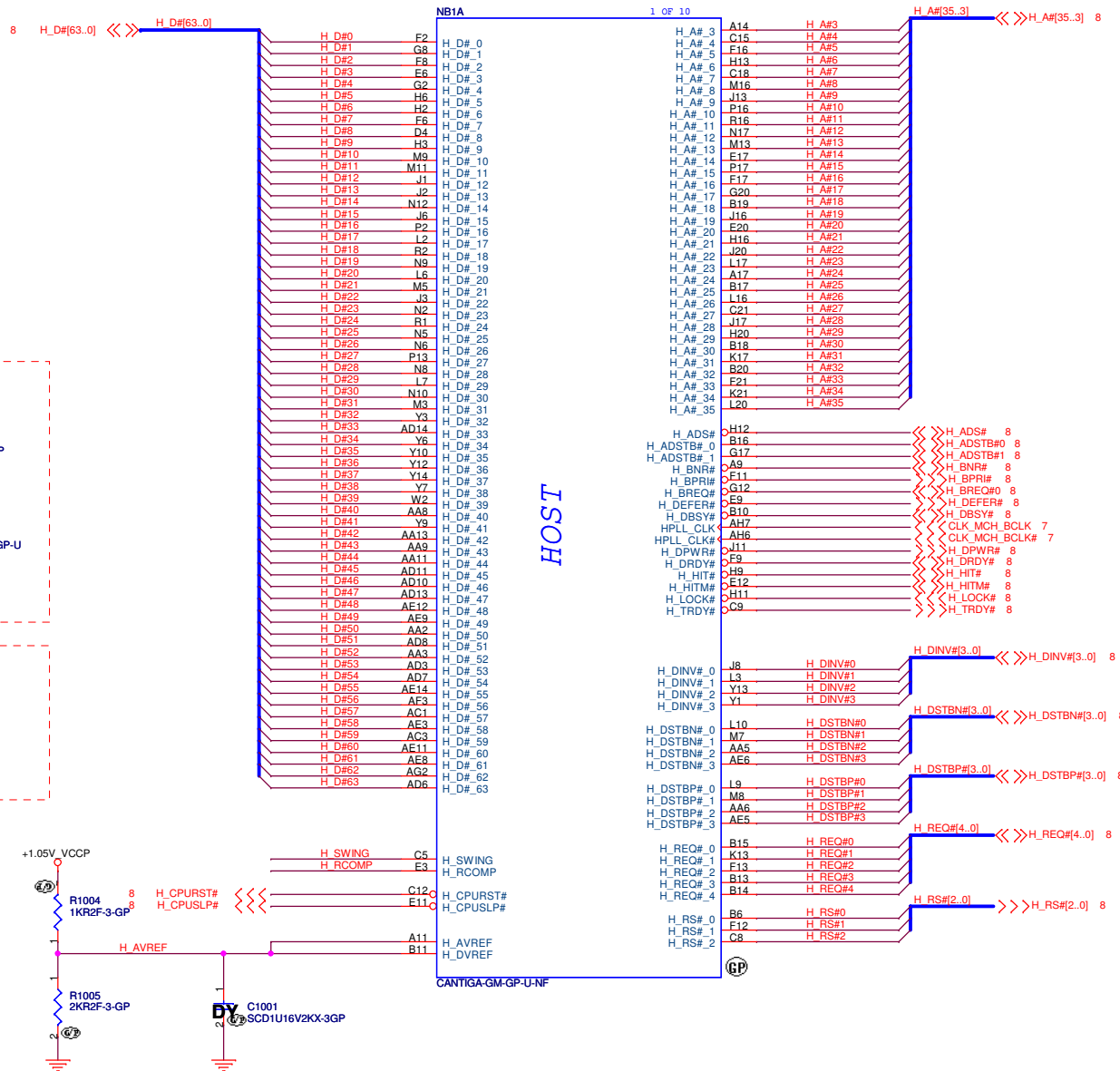
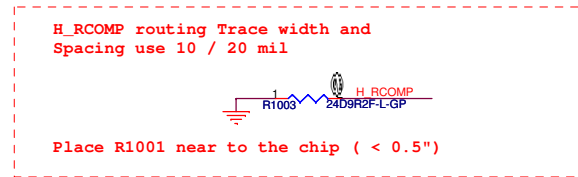
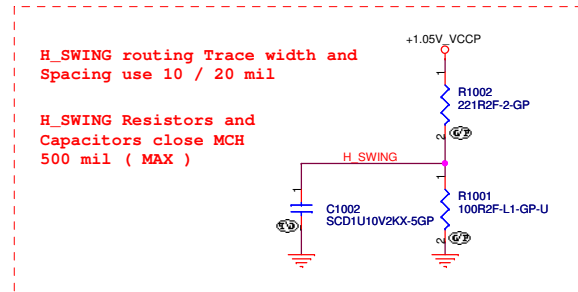
<Core Design>

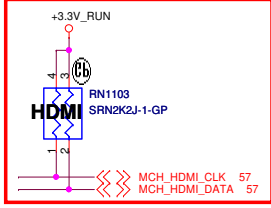
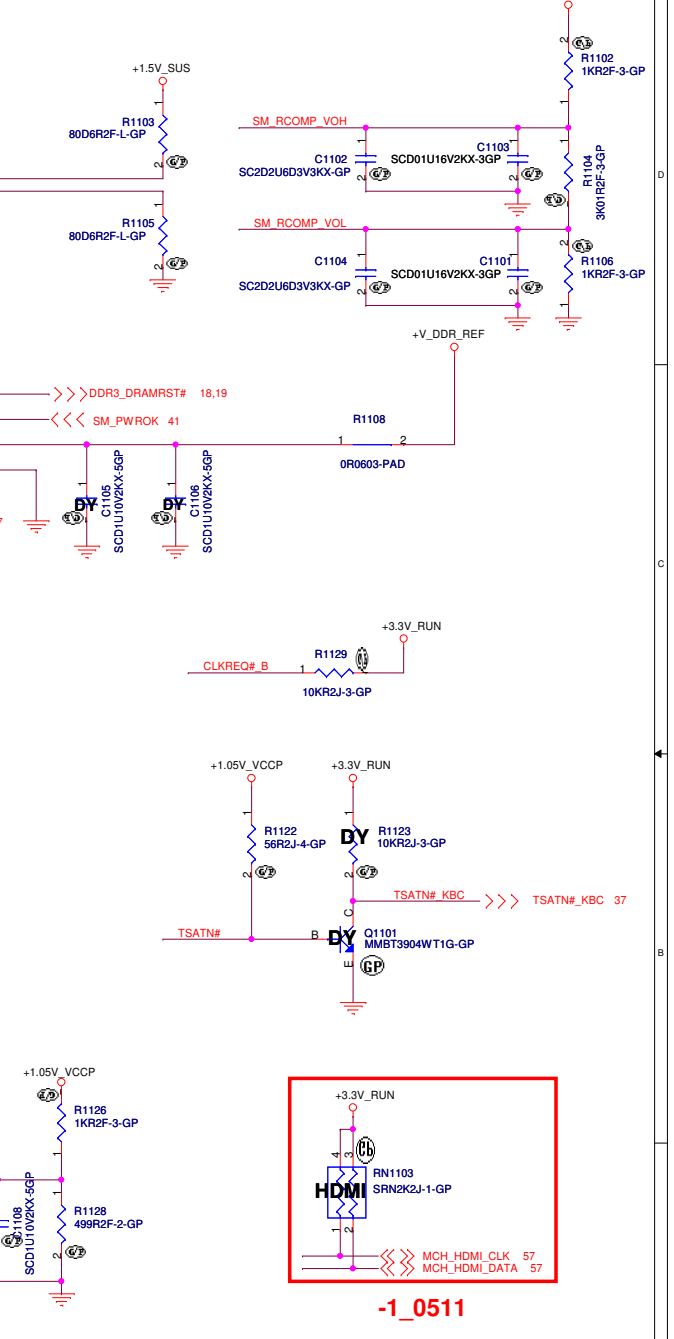
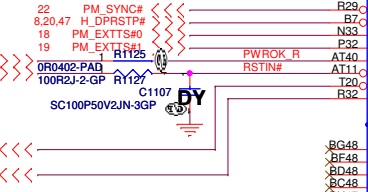
DELL		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
Size Custom	Document Number DJ2 Montevina UMA	Rev X0	
Date: Friday, May 28, 2010	Sheet 6	of	88

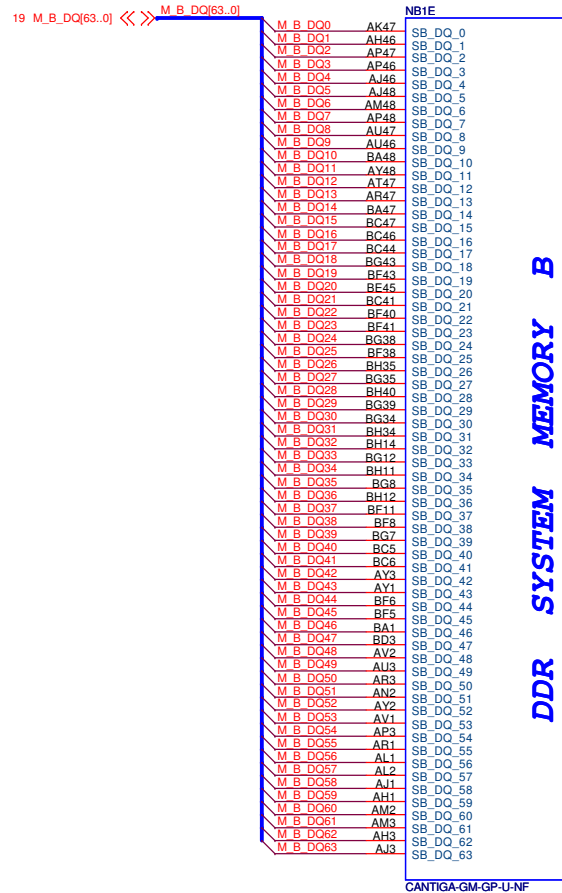
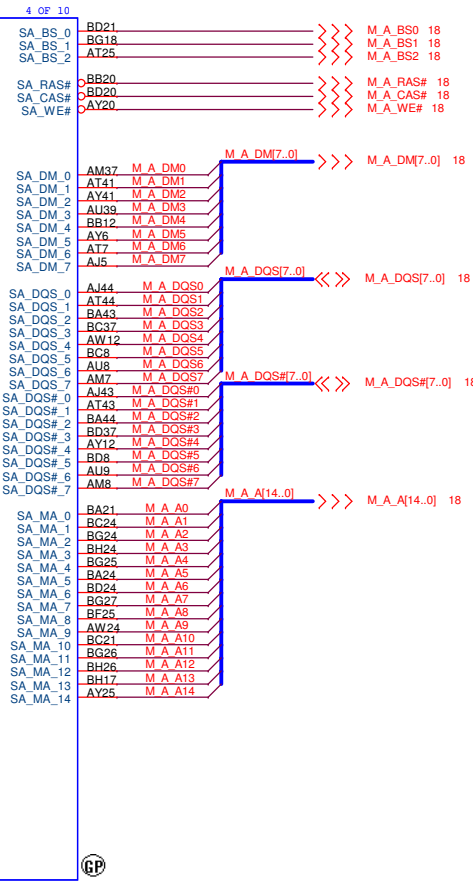
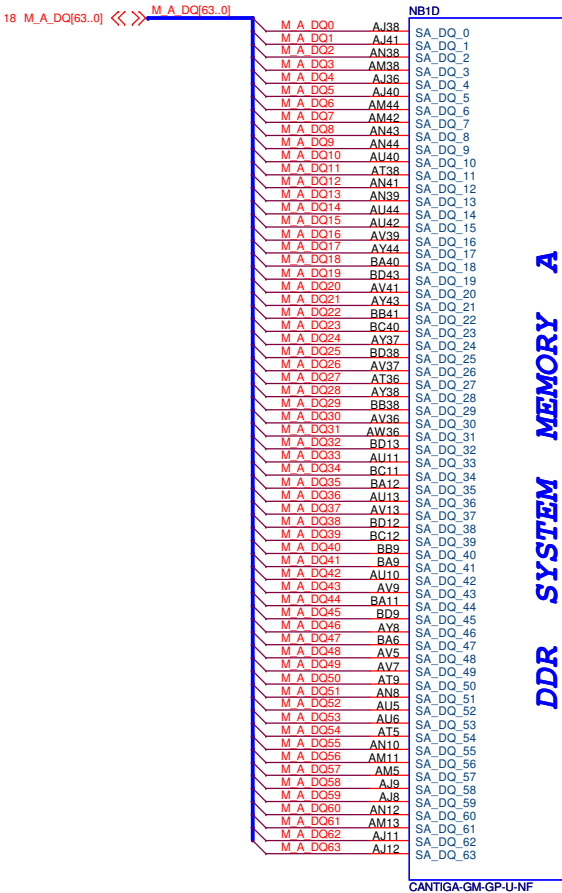












<Core Design>

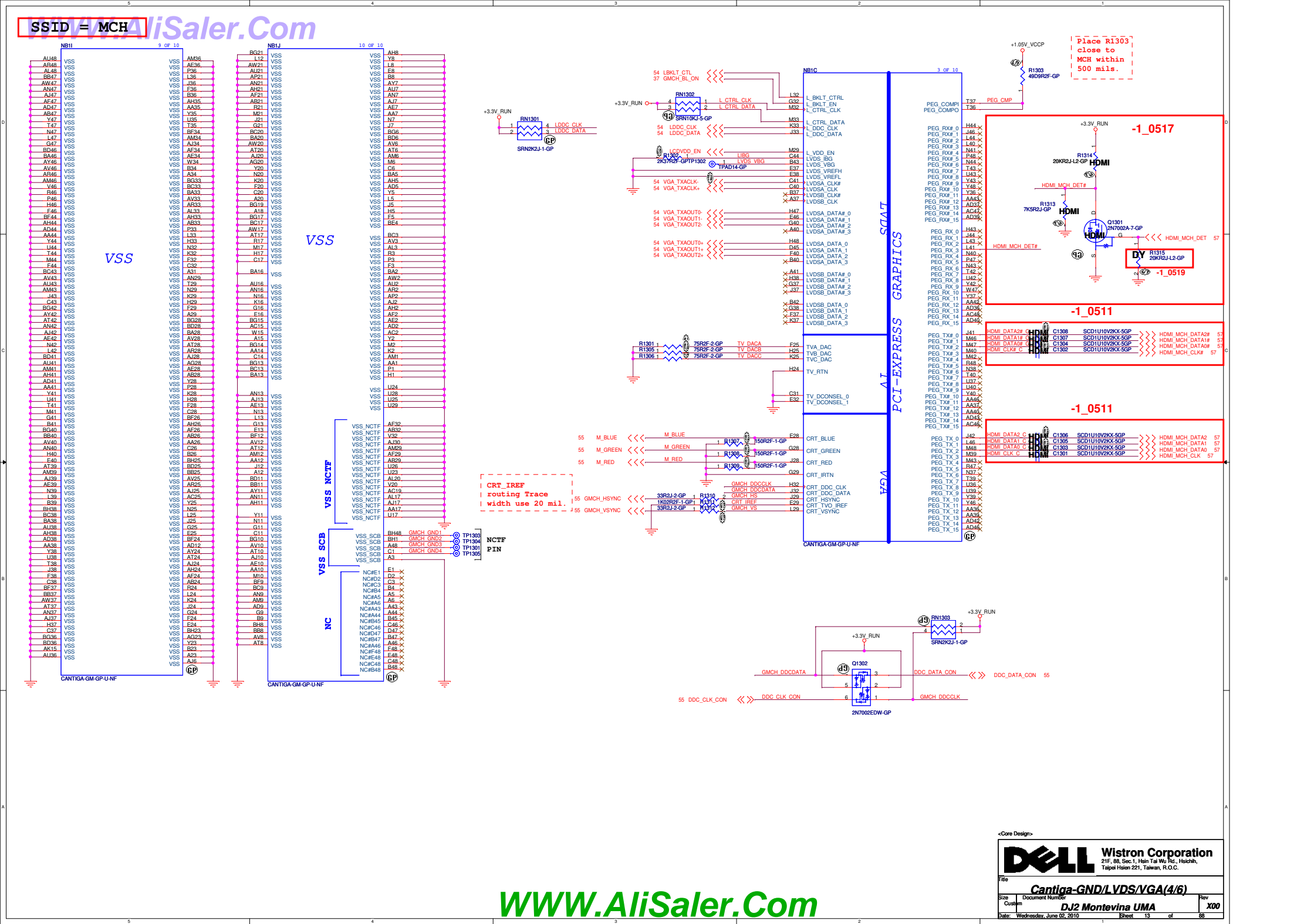
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

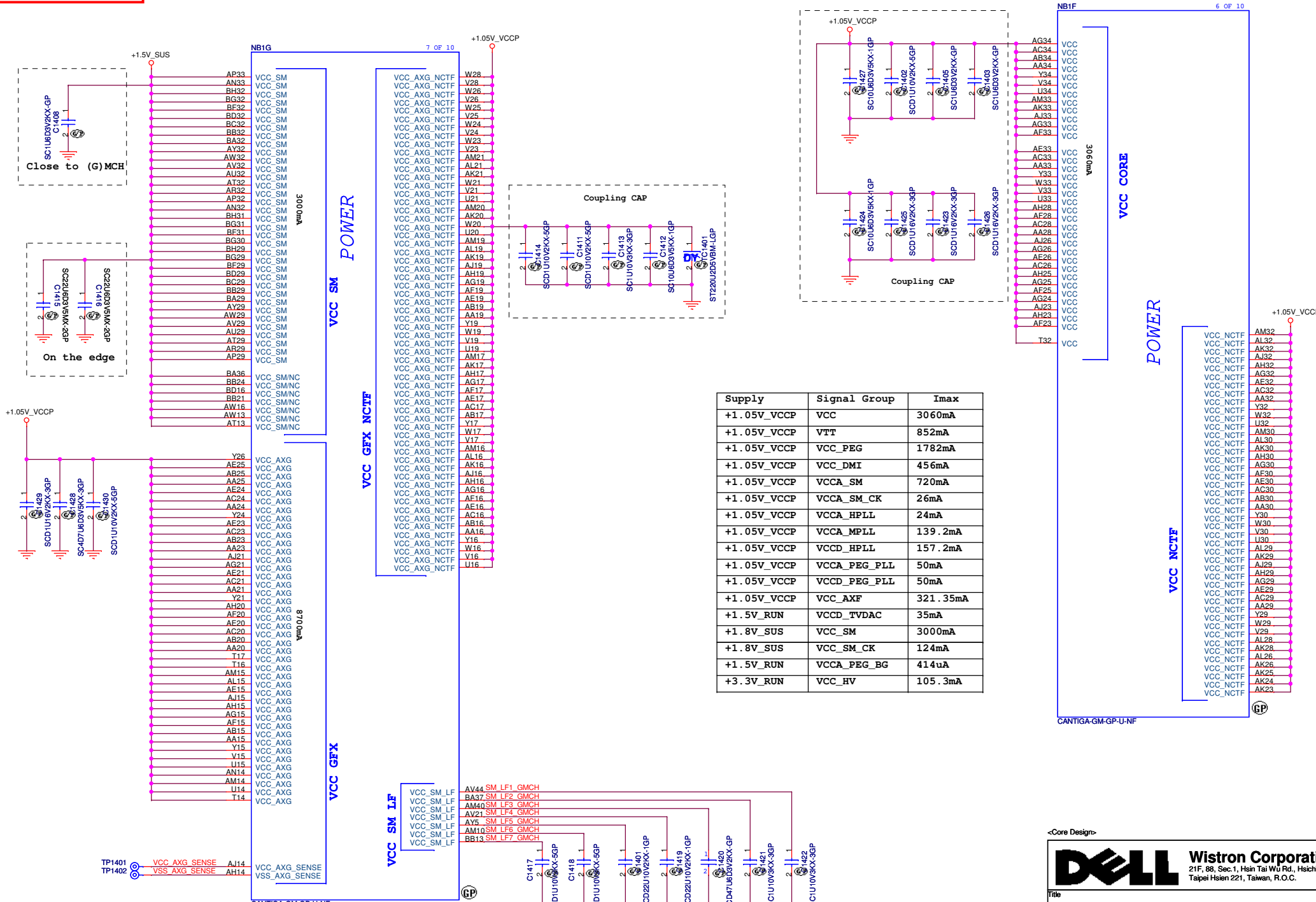
Title
Cantiga-DDR(3/6)

Size Document Number
Custom **DJ2 Montevina UMA**

Date: Wednesday, June 02, 2010 Sheet 12 of 88

Rev **X00**





Supply	Signal Group	Imax
+1.05V_VCCP	VCC	3060mA
+1.05V_VCCP	VTT	852mA
+1.05V_VCCP	VCC_PEG	1782mA
+1.05V_VCCP	VCC_DMI	456mA
+1.05V_VCCP	VCCA_SM	720mA
+1.05V_VCCP	VCCA_SM_CK	26mA
+1.05V_VCCP	VCCA_HPLL	24mA
+1.05V_VCCP	VCCA_MPLL	139.2mA
+1.05V_VCCP	VCCD_HPLL	157.2mA
+1.05V_VCCP	VCCA_PEG_PLL	50mA
+1.05V_VCCP	VCC_AXF	321.35mA
+1.5V_RUN	VCCD_TVDAC	35mA
+1.8V_SUS	VCC_SM	3000mA
+1.8V_SUS	VCC_SM_CK	124mA
+1.5V_RUN	VCCA_PEG_BG	414uA
+3.3V_RUN	VCC_HV	105.3mA

Core Design

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga-Power(5/6)**

Size: **Custom** Document Number: **DJ2 Montevina UMA** Rev: **X00**

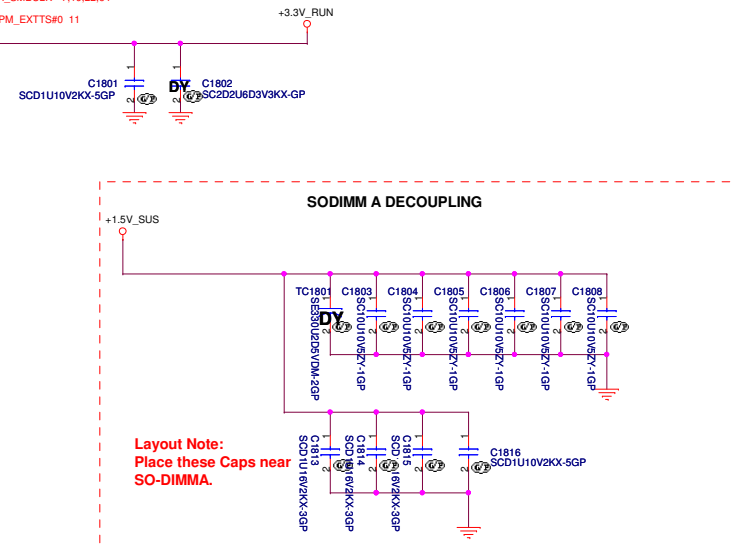
Date: Saturday, May 29, 2010 Sheet 14 of 88



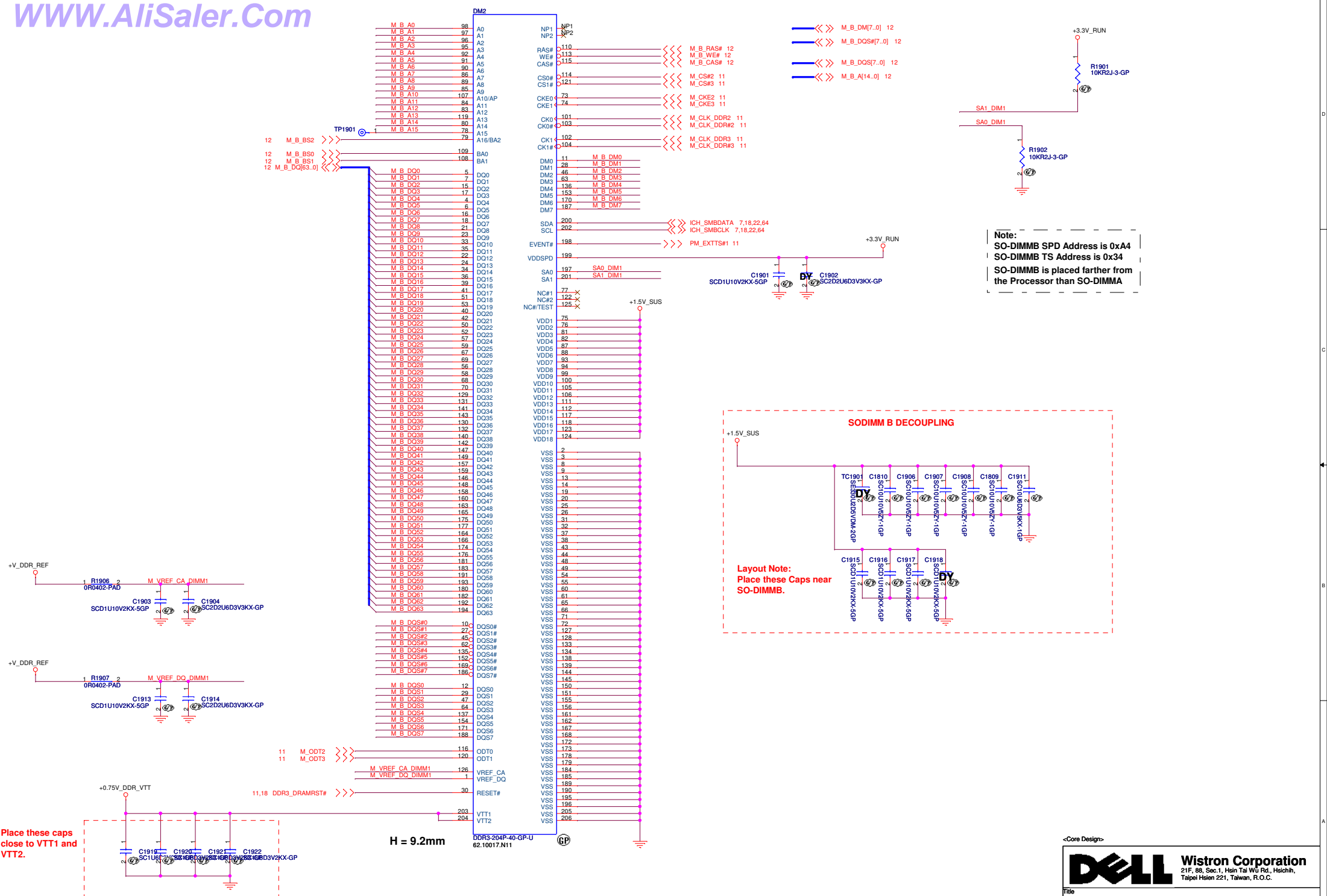


Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

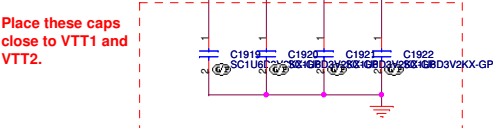
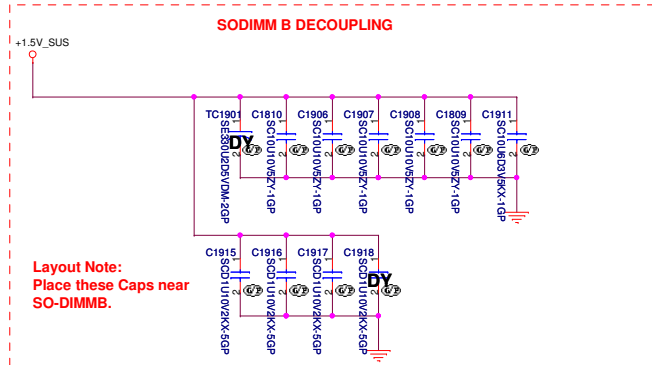
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

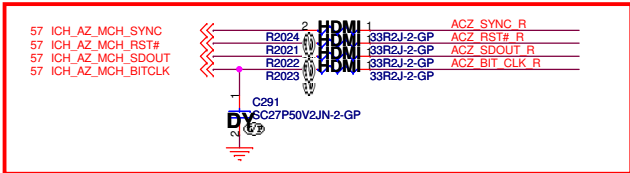
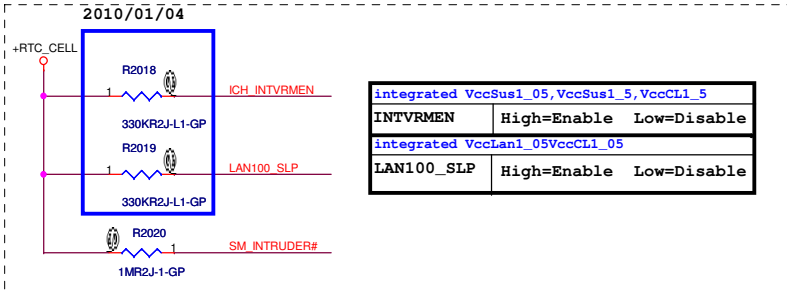
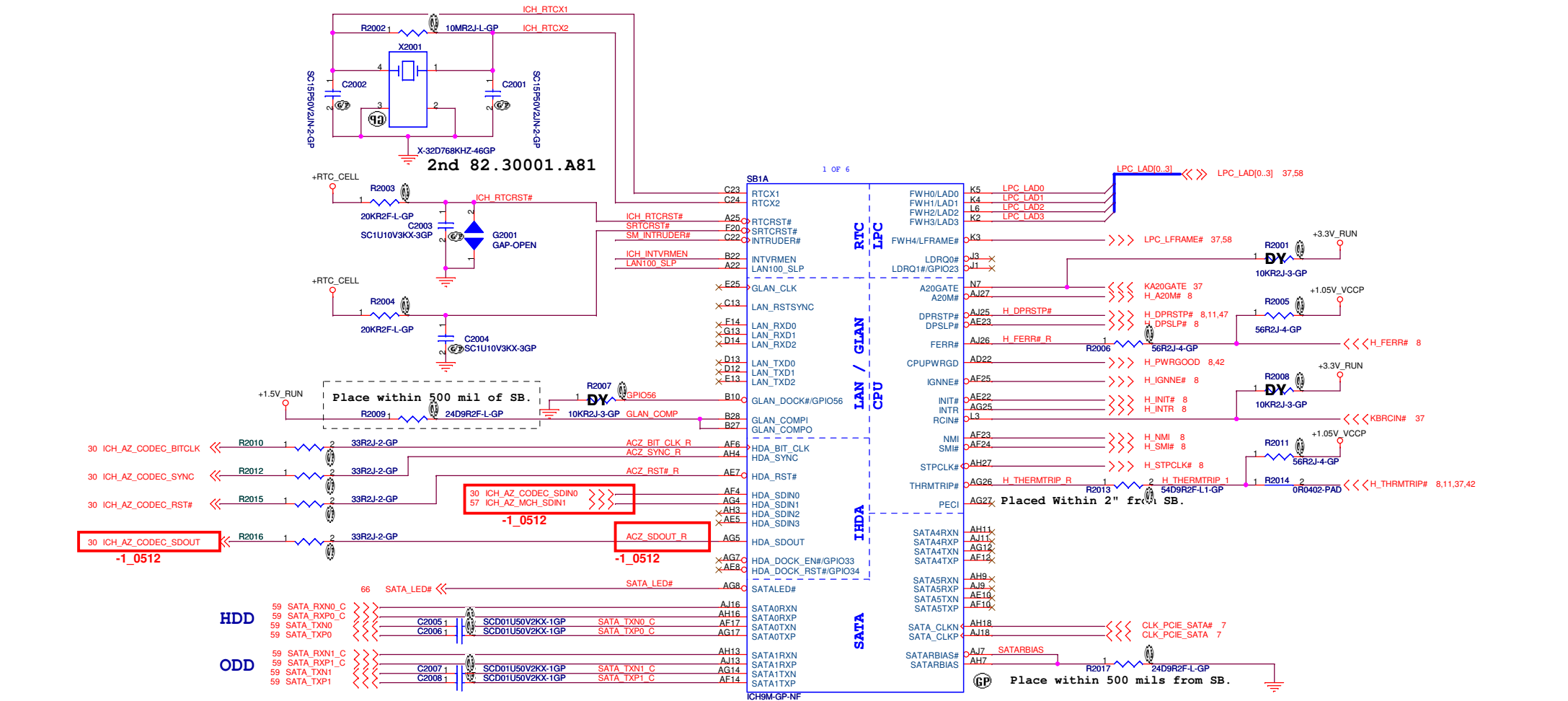


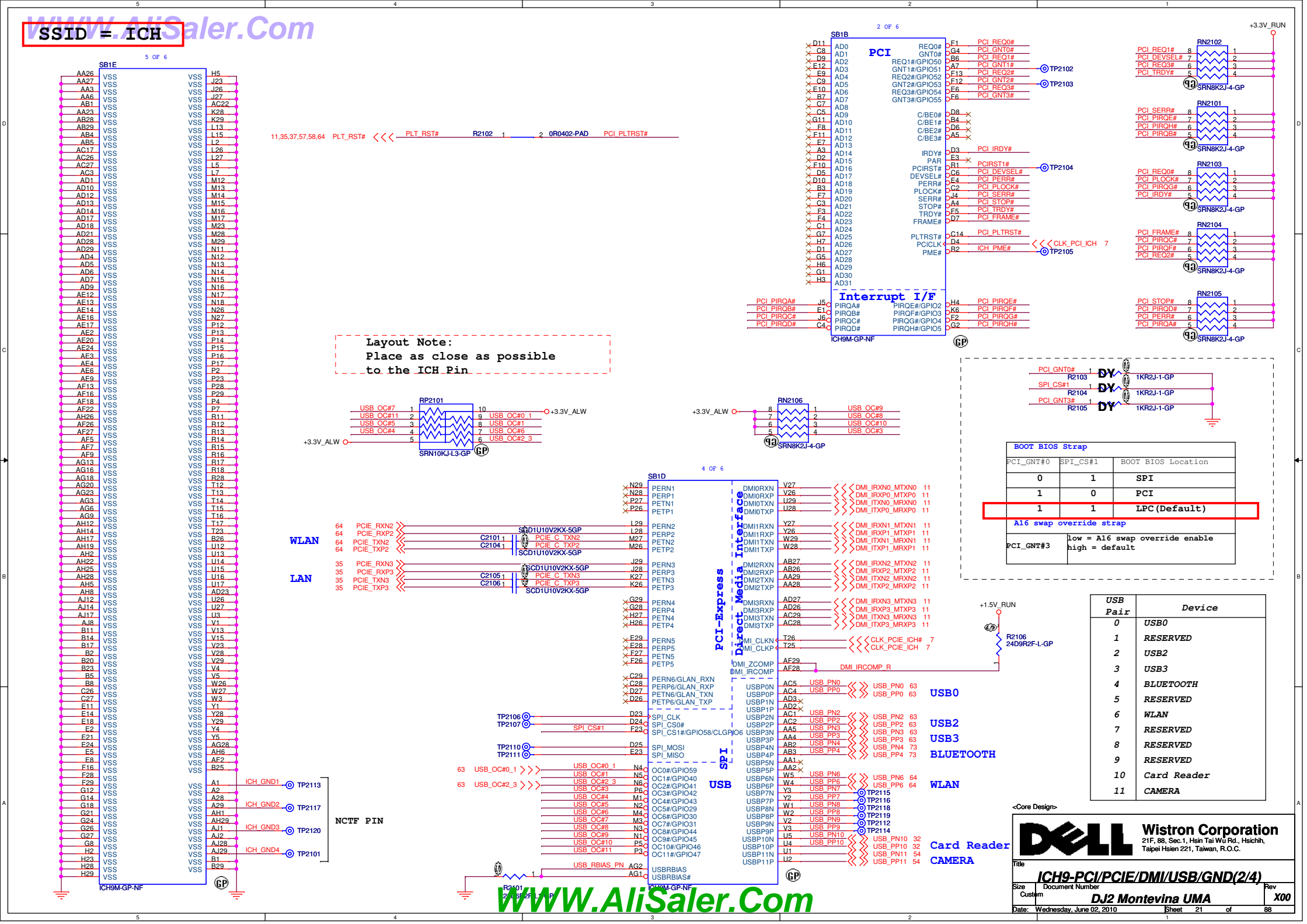
Layout Note
Place these
SO-DIMMA.

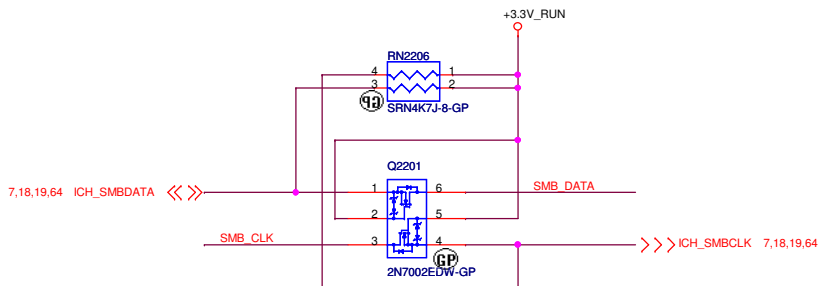
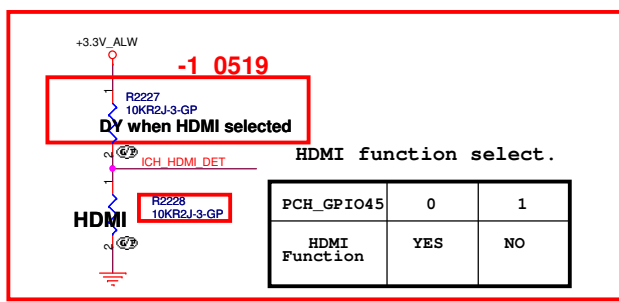
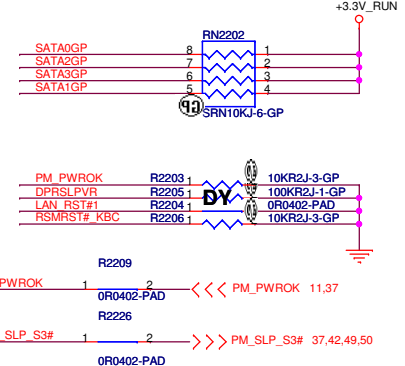
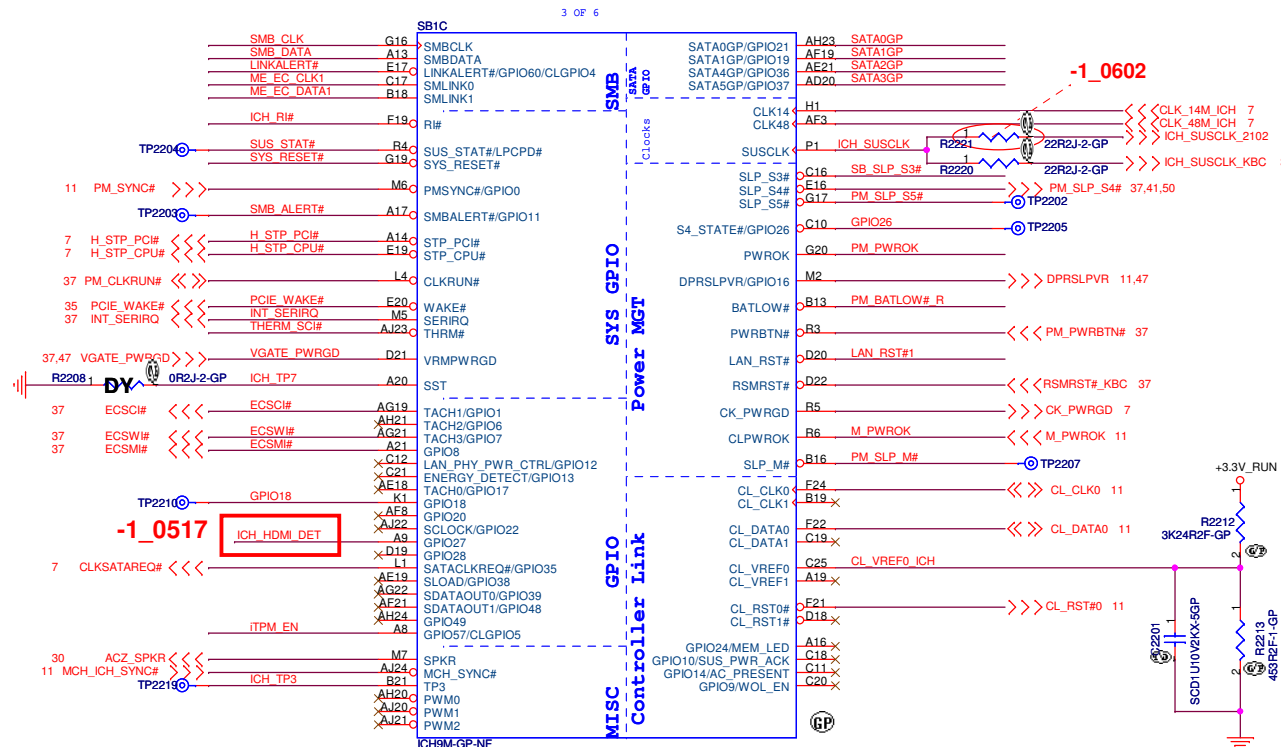
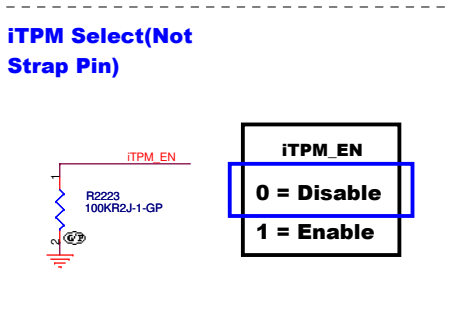
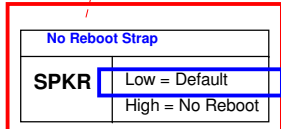
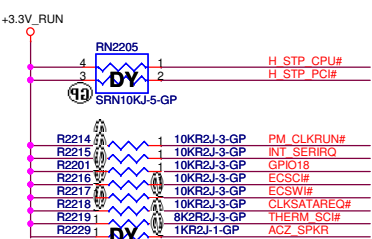
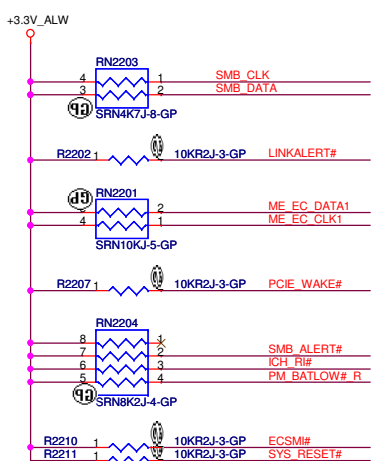


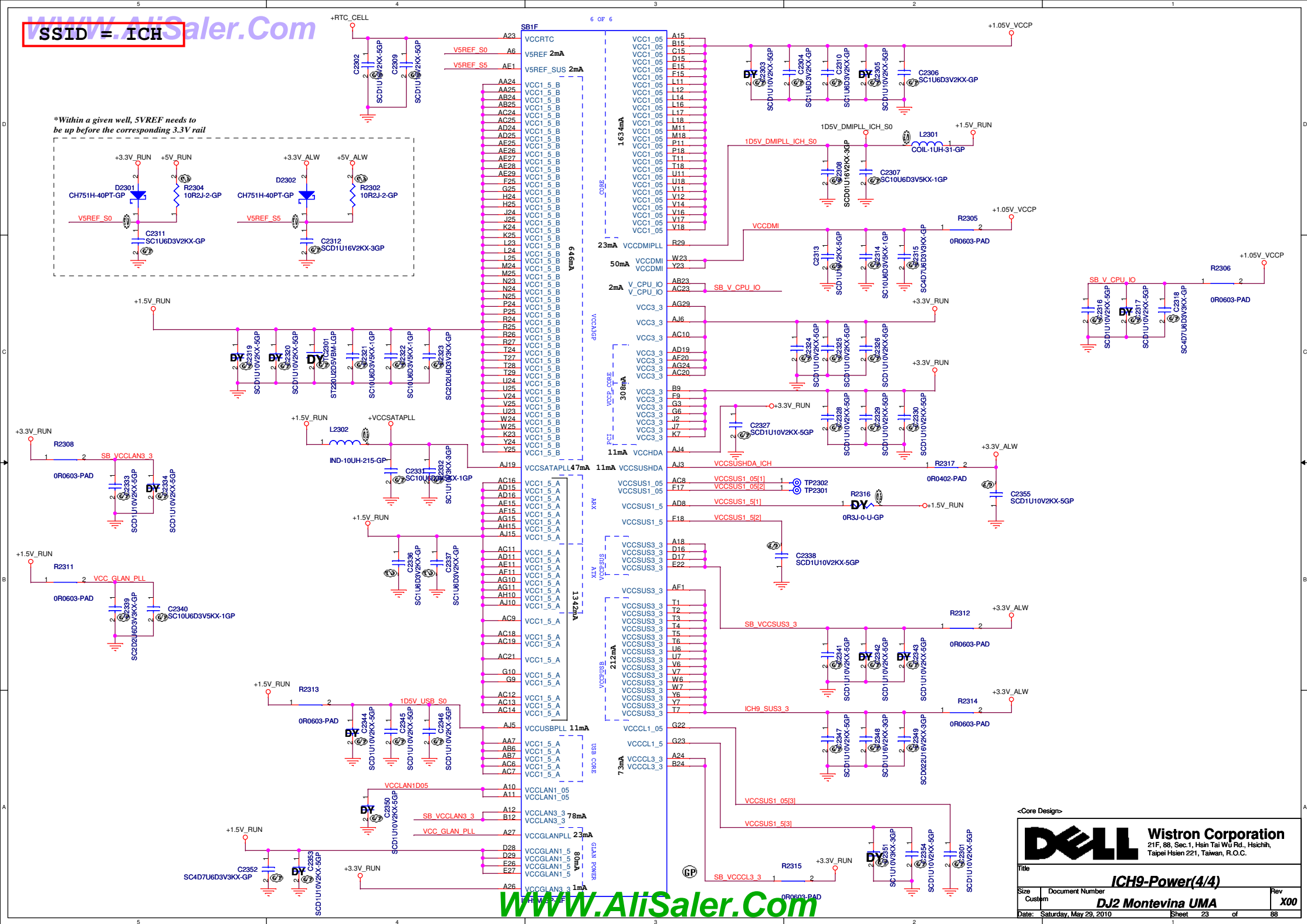
Note:
SO-DIMM SPD Address is 0xA4
SO-DIMM TS Address is 0x34
SO-DIMM is placed further from
the Processor than SO-DIMMA





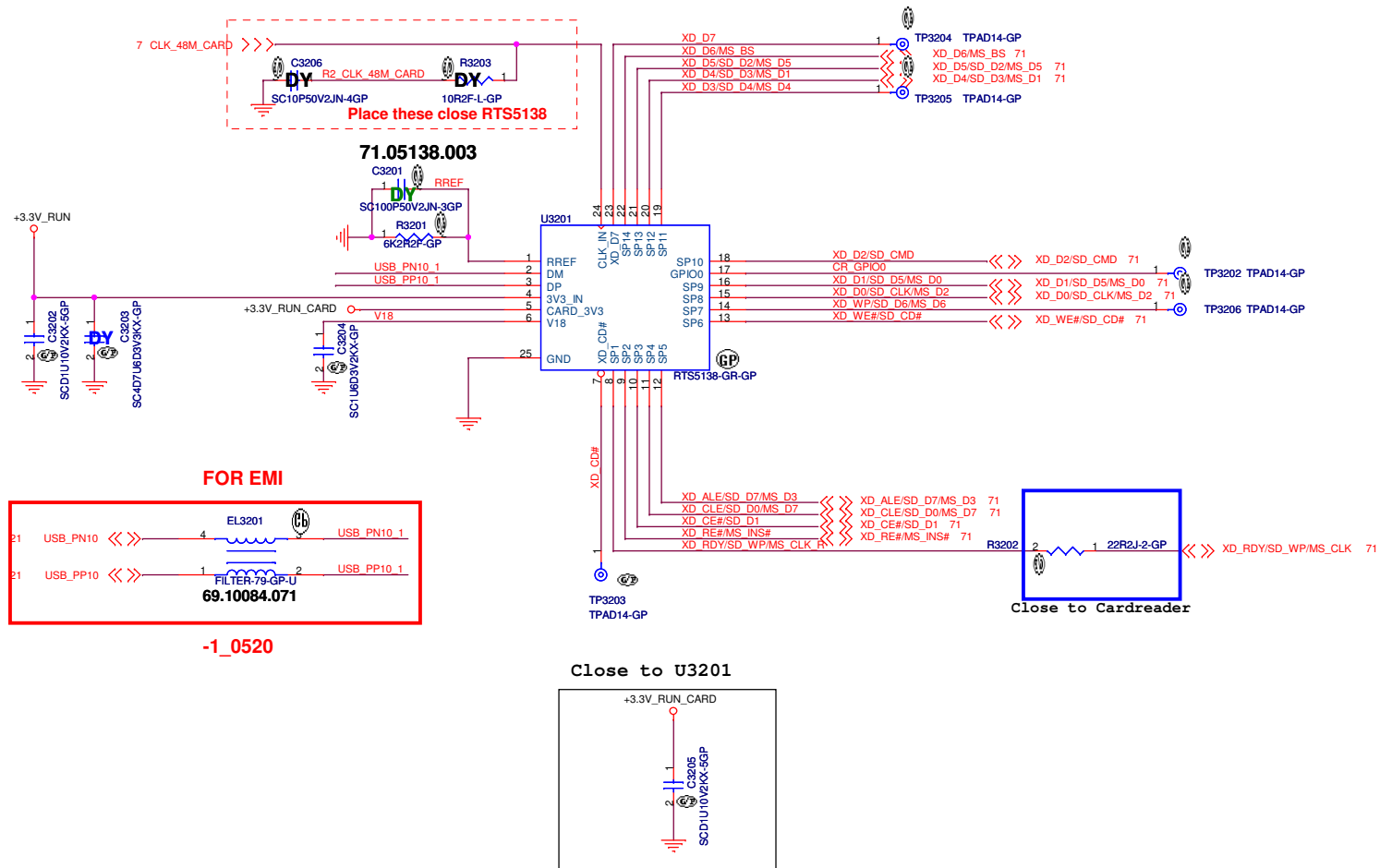






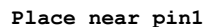
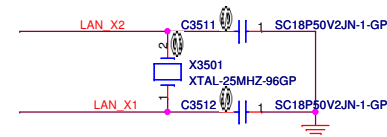


SSID = SDIO

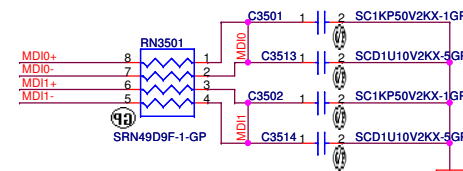


<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Card Reader-RTS5138					
Size	Document Number	Rev			
Custom	DJ2 Montevina UMA				X00
Date:	Wednesday, June 02, 2010	Sheet	32	of	88



-1 0521

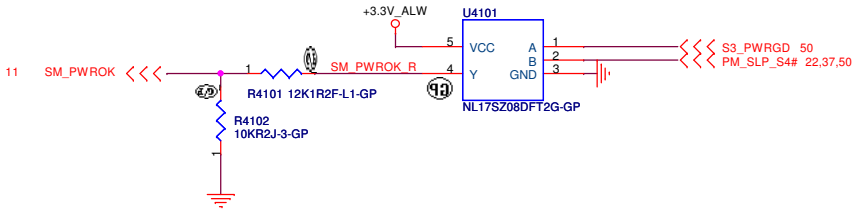


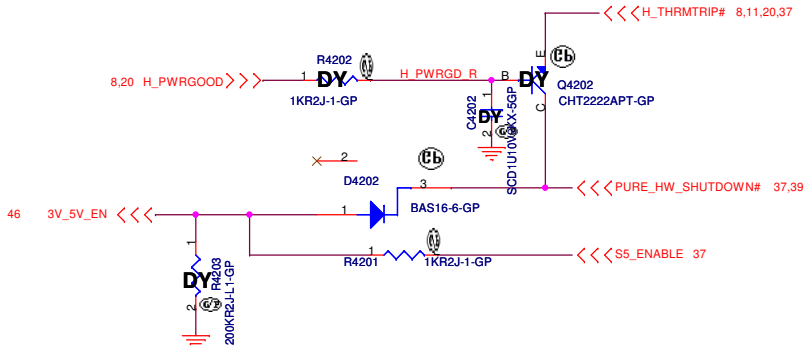
WWW.AliSaler.Com



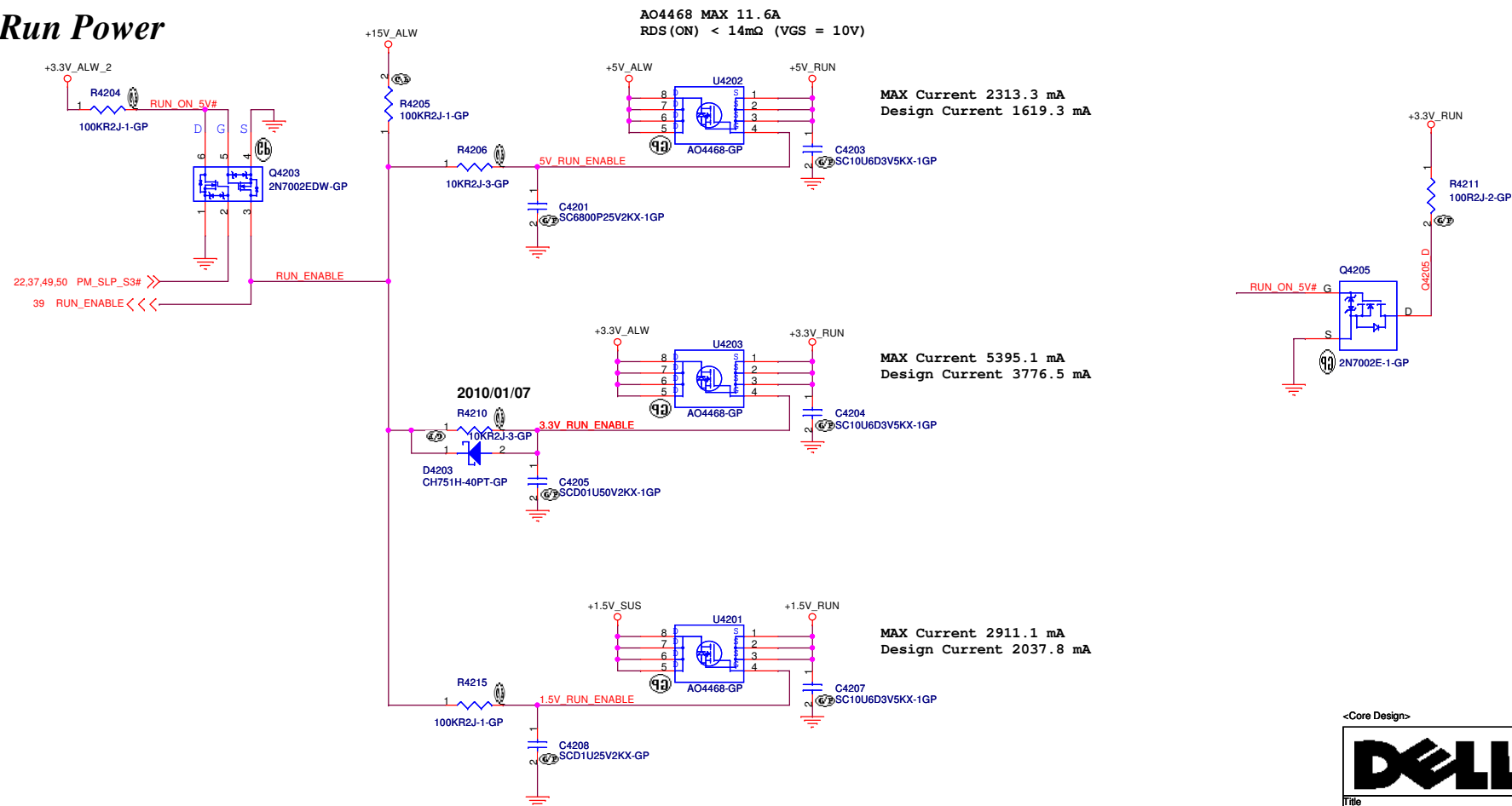


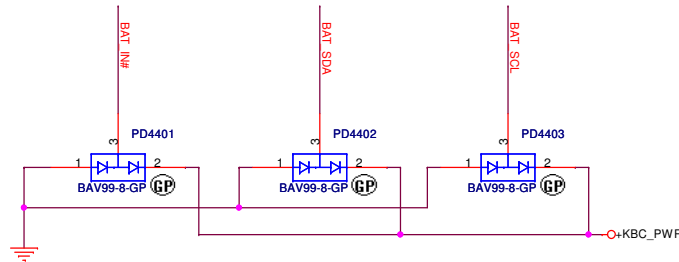
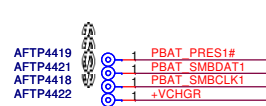
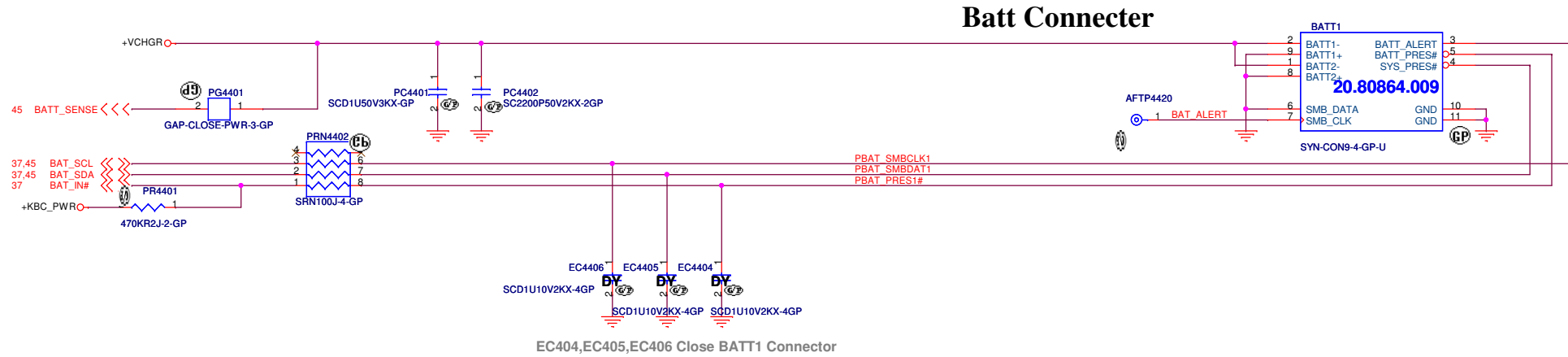
SSID = Reset.Suspend





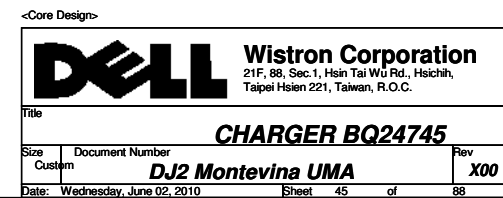
Run Power



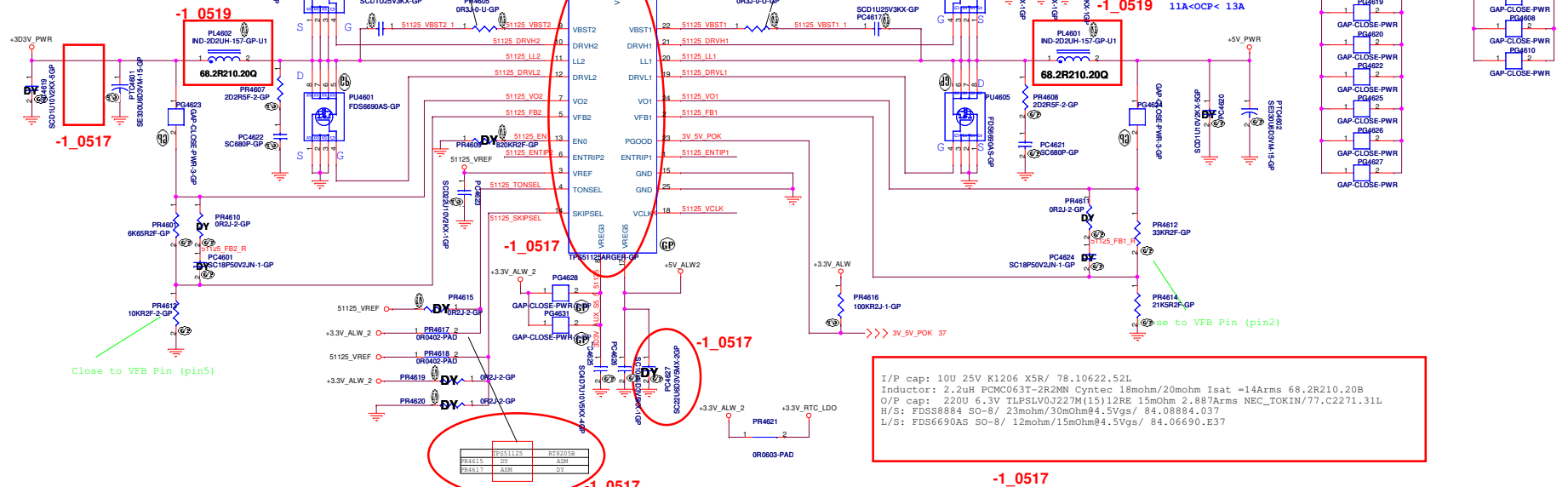


<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		BATT CONN	
		Title	
Size A3	Document Number DJ2 Montevina UMA	Rev X00	
Date: Wednesday, June 02, 2010		Sheet 44 of 88	



Design Current = 7.6A
11.95A < OCP < 14.12A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R22M Cynotec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEP5L220107M(45)R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

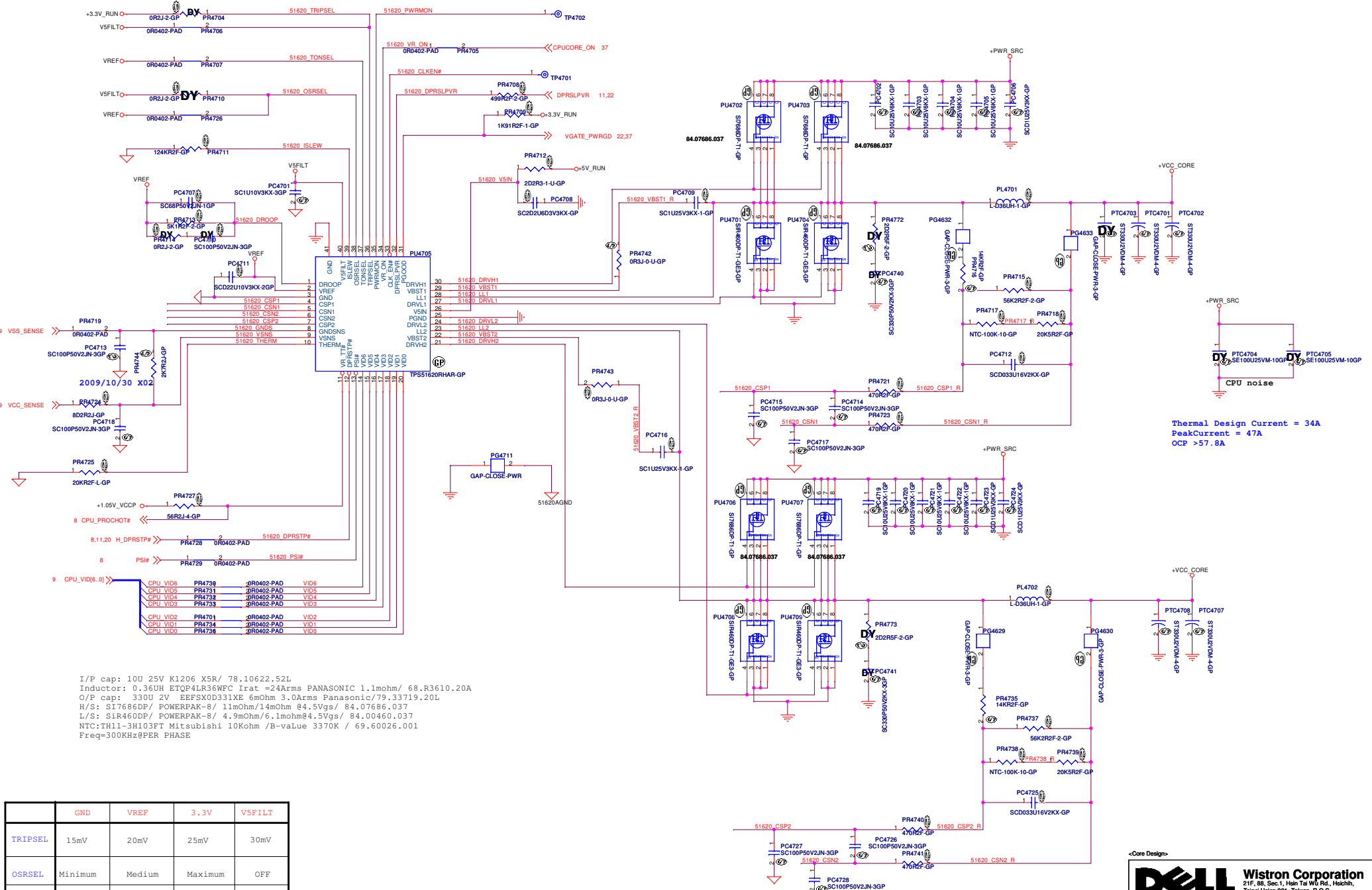
EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC063T-2R22M Cynotec 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap: 220U 6.3V TEP5L220107M(45)R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8884 SO-8/ 23mohm/30mohm@4.5Vgs/ 84.08884.037
L/S: FDS6690AS SO-8/ 12mohm/15mohm@4.5Vgs/ 84.06690.E37

<Core Design>

DELL Wistron Corporation			
21F, 8B, Sec 1, Hsin Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.			
File: TPS51125_5V/3D3V			
Size A2	Document Number	Rev	X00
DJ2 Montevina UMA			
Date: Wednesday, June 02, 2010	Sheet 46	of 88	

SSID = CPU.Regulator



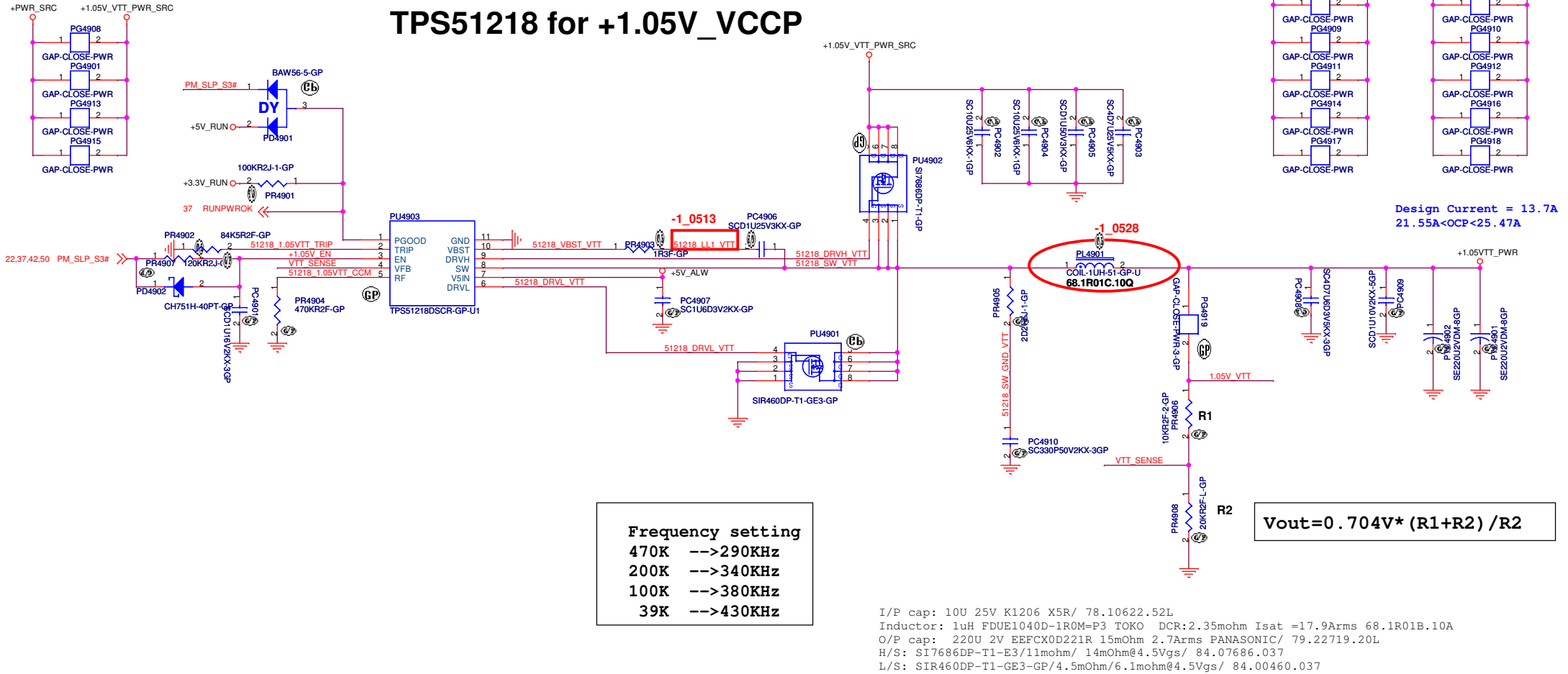
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taiwan, R.O.C.

DELL

CPU Vcore Power

Size: Custom
 Document Number: D.J2 Montevina UMA
 Date: Wednesday, June 02, 2010
 Sheet: 47 of 88

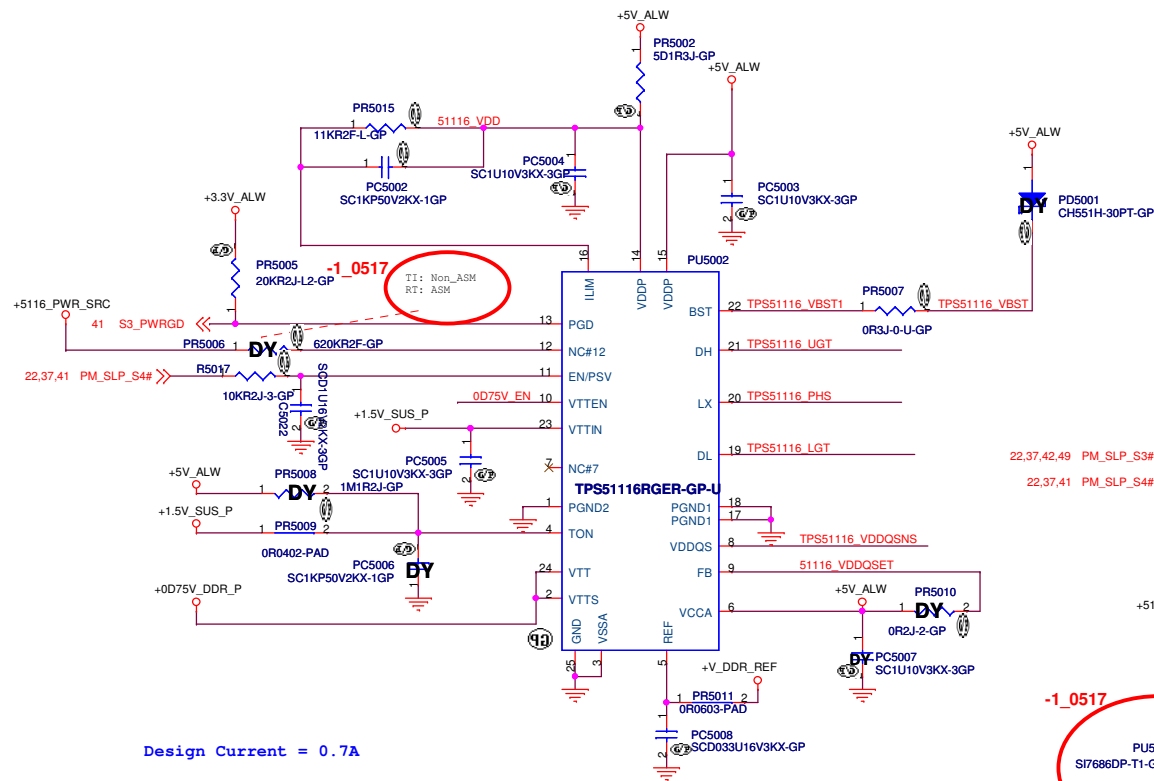
SSID = PWR.Plane.Regulator_1p05v



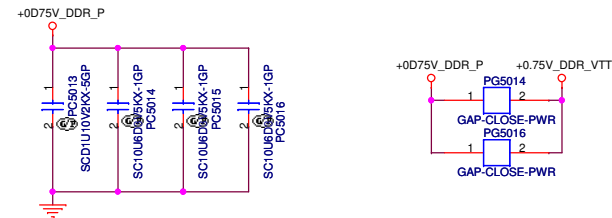
<Core Design>

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title TPS51218 +1.05V VCCP			
Size Custom	Document Number DJ2 Montevina UMA	Rev X00	
Date: Wednesday, June 02, 2010	Sheet 49	of 88	

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



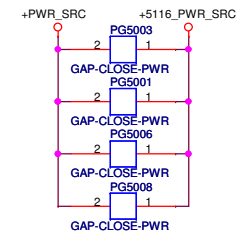
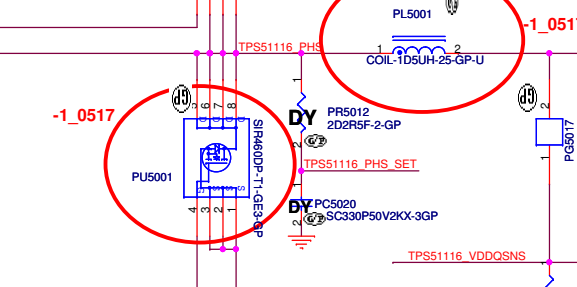
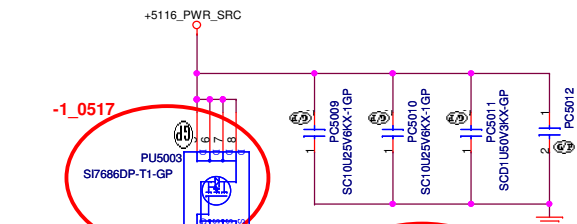
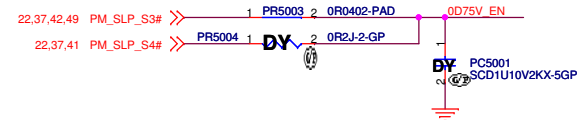
Design Current = 0.7A



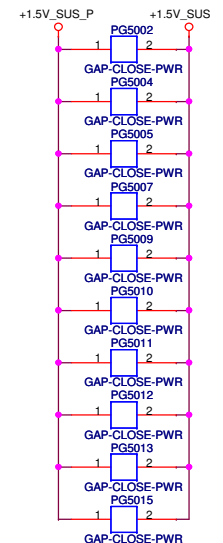
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTRF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH FDVE1040-1R5M=P3 DCR:4.6mohm Isat =13.7Arms TOKO/ 68.1R51A.10G
O/P cap: 330U 2.5V EEFCCO3E310R 15mOhm 2.7Arms PANASONIC/ 79.3371V.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SI4460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq-->400KHz

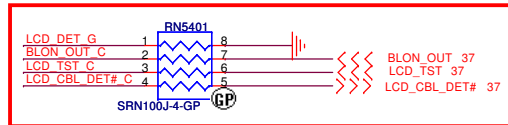


Design Current = 9.82A
15.43A < OCP < 18.24A



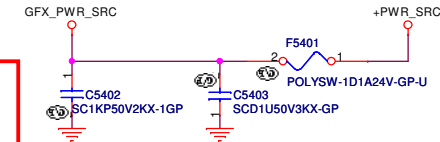
Close to VFB Pin (pin5)

<div> <div>  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> </div> </div>			
Title			
TPS51116 +1.5V SUS			
Size	Document Number	Rev	
Custom	DJ2 Montevina UMA	X00	
Date:	Wednesday, June 02, 2010	Sheet 50 of	88



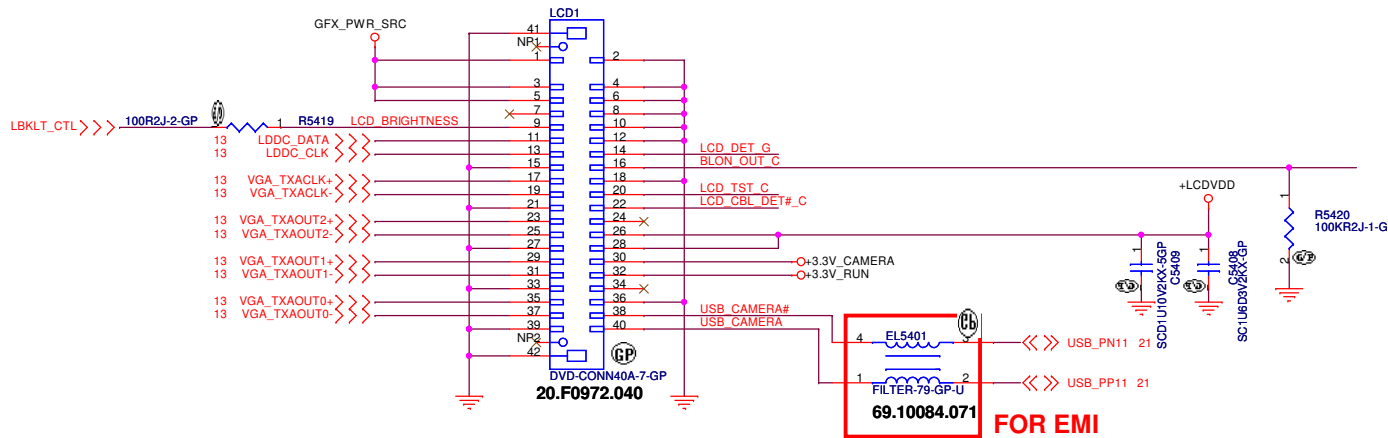
-1_0526
SWAP for Layout

INVERTER POWER



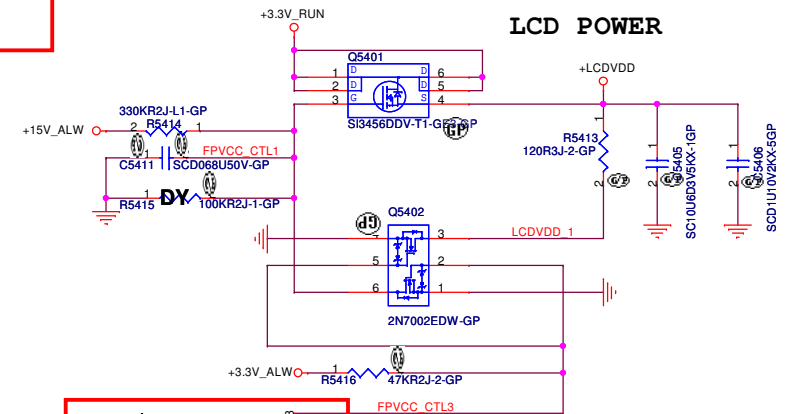
SSID = VIDEO

LVDS CONNECTOR



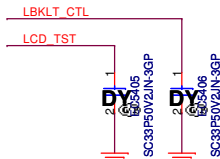
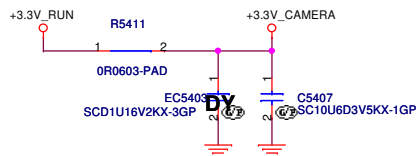
-1_0512

LCD POWER



-1_0525

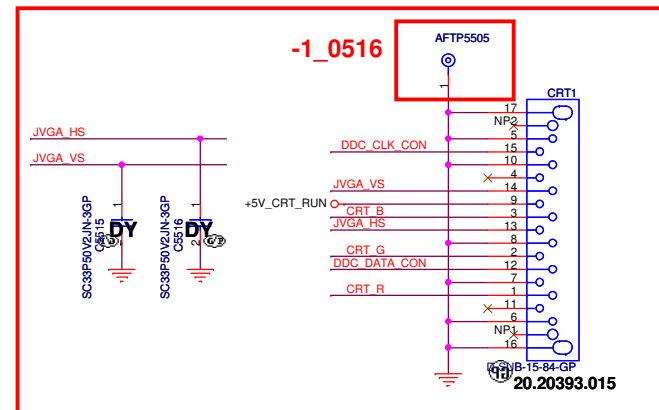
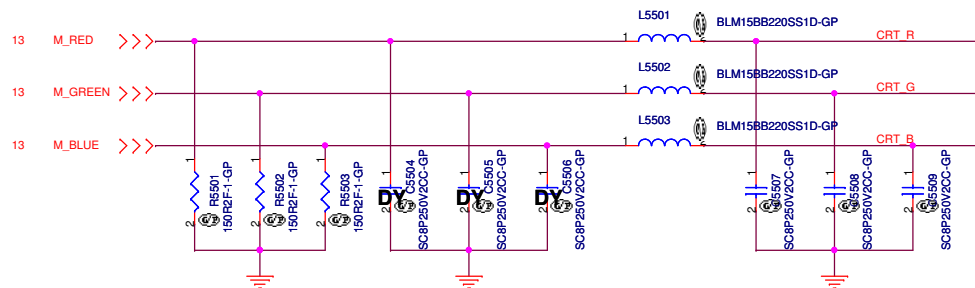
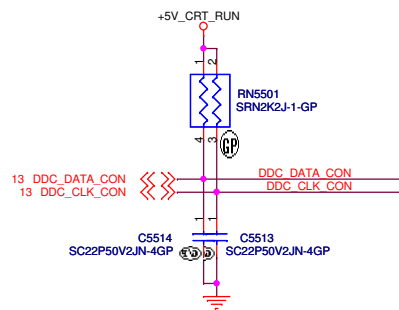
Camera Power



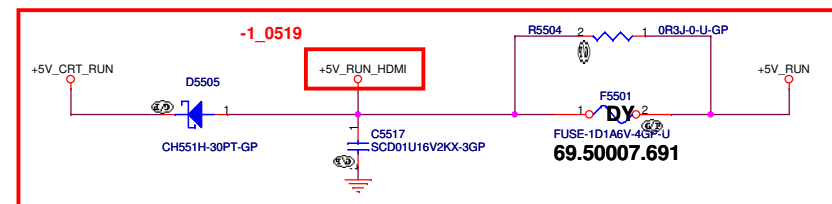
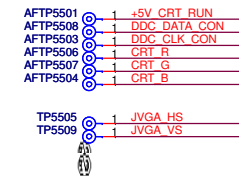
For EMI request

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

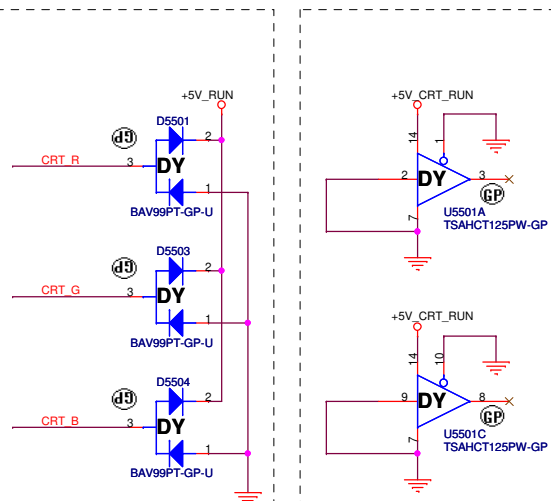
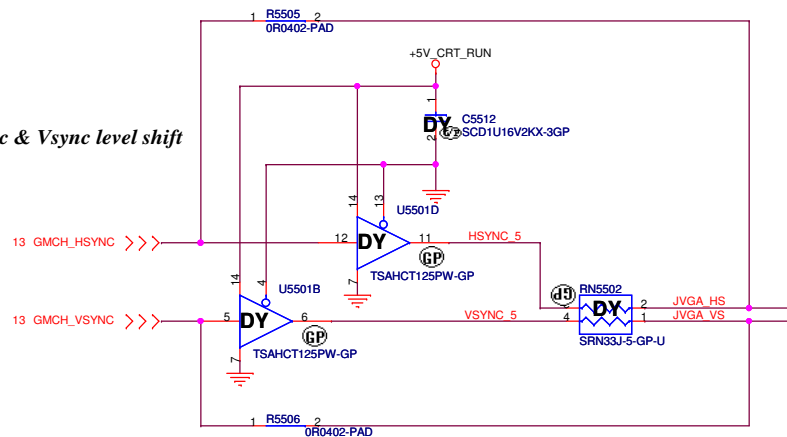


-1_0511



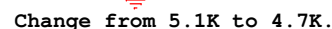
-1_0511 for safety option

Hsync & Vsync level shift



<Core Design>

HDMI CONN



```
1st Parade 71.P8101.003
2nd NXP 71.03360.A0K
3rd Pericom 71.03411.D03
```

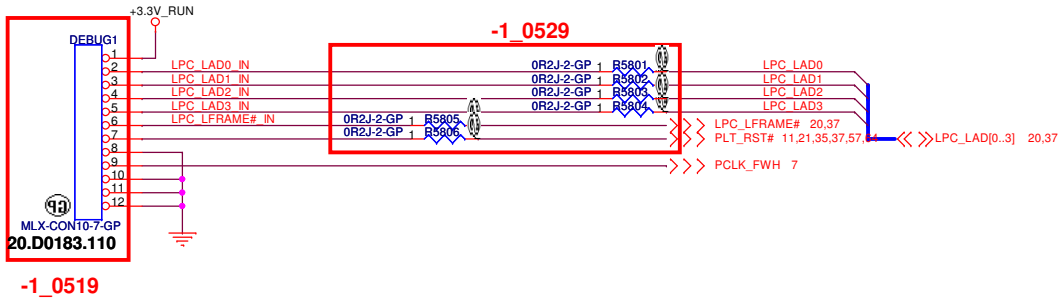


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **HDMI Level Shift/ Connector**

Size A3	Document Number DJ2 Montevina UMA	Rev X00
Date: Wednesday, June 02, 2010	Sheet 57 of 88	

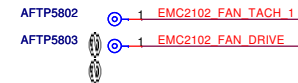
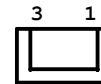
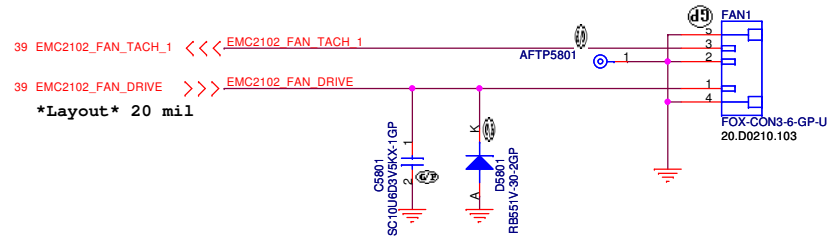
SSID = User.Interface



-1_0529

SSID = Thermal

Fan Connector



<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

ITP/Fan Connector

Size
A3

Document Number

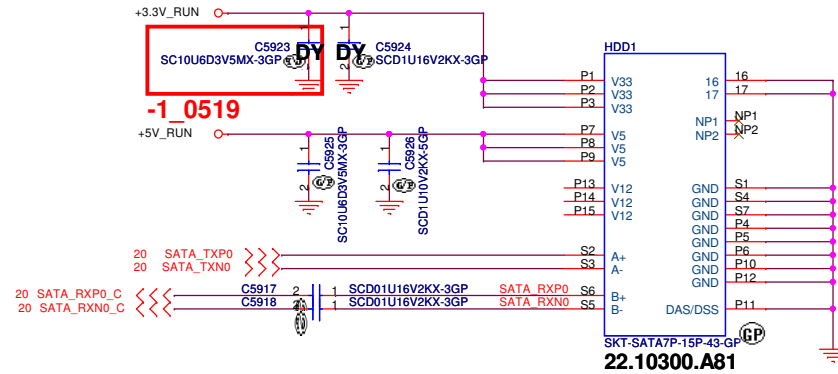
DJ2 Montevina UMA

Rev
X00

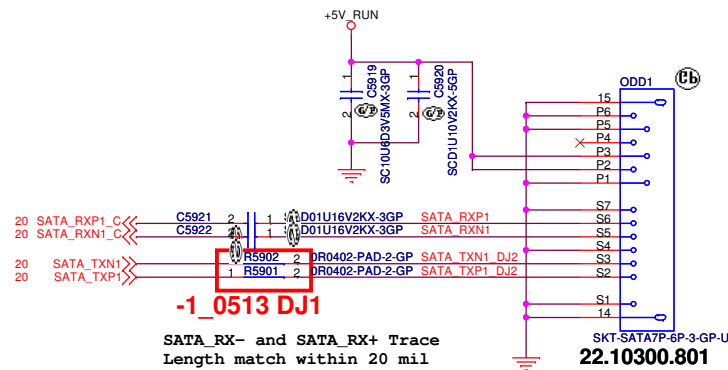
Date: Wednesday, June 02, 2010

Sheet 58 of 88

SATA HDD Connector



ODD Connector



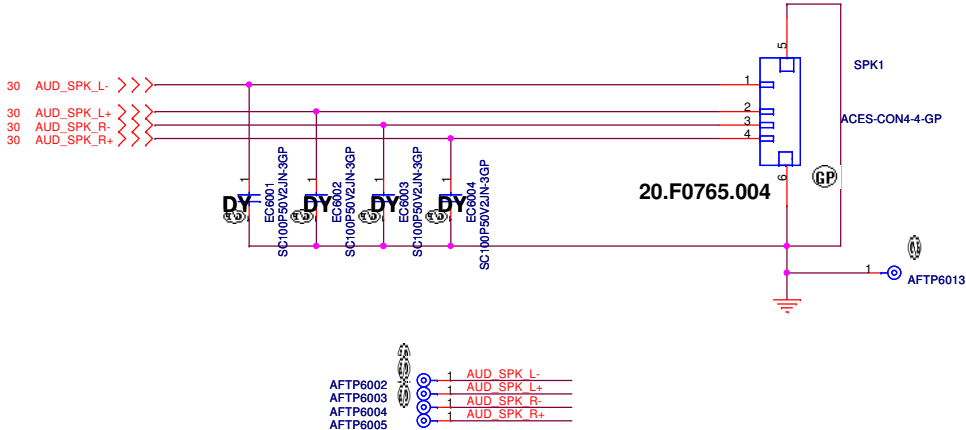
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

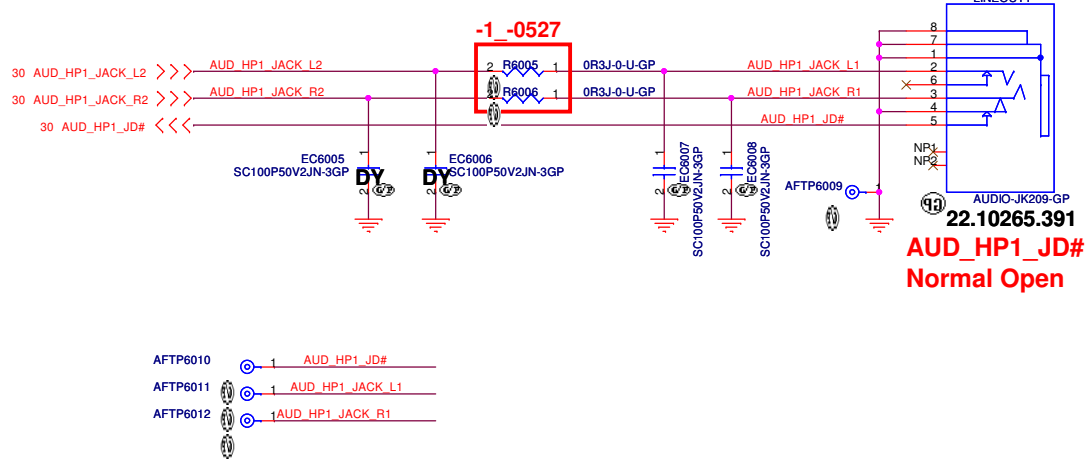
Title			HDD/ODD	
Size	Document Number	Rev		
A3	DJ2 Montevina UMA	X00		
Date:	Wednesday, June 02, 2010	Sheet	59	of 88

SSID = AUDIO

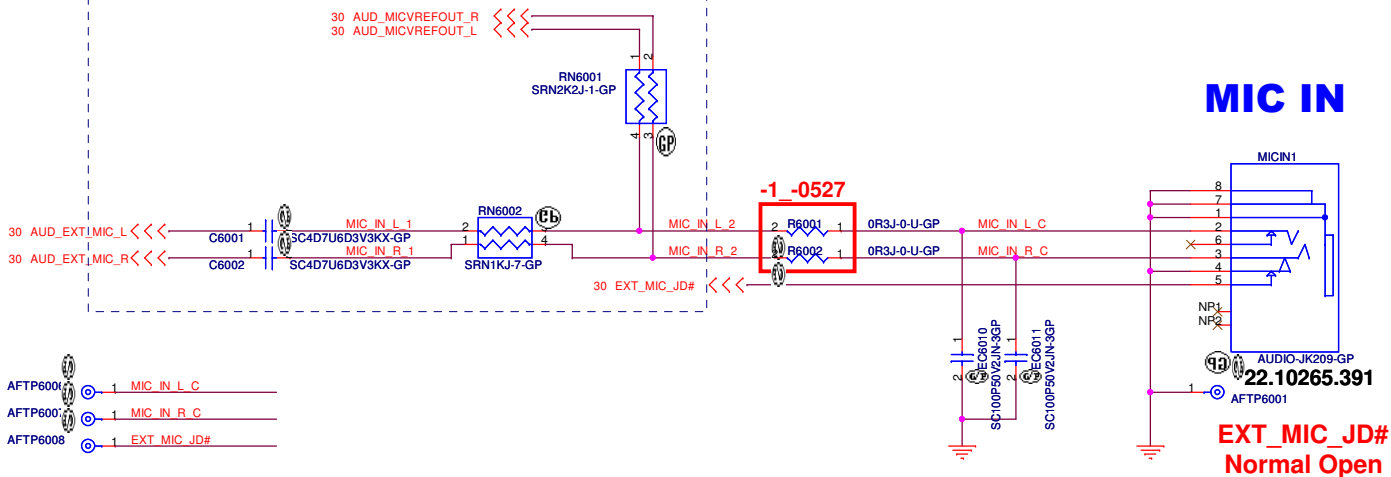
Speaker Connector



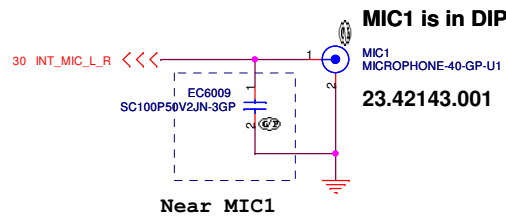
LINE1 OUT



Plase thise parts near codec

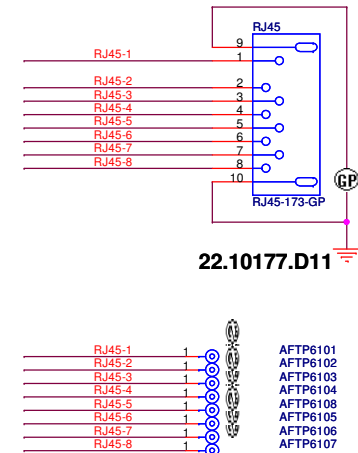


Internal Microphone



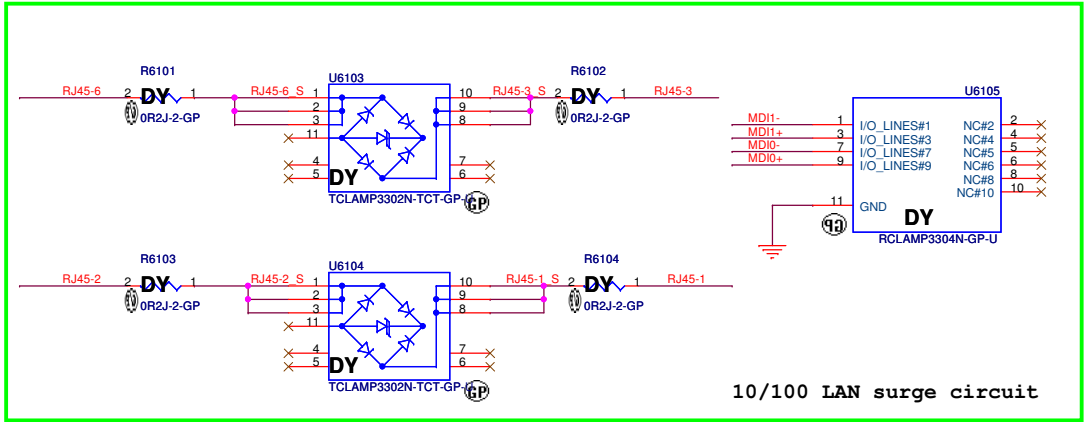
-1_0601
Remove for EMI

RJ45 Connector



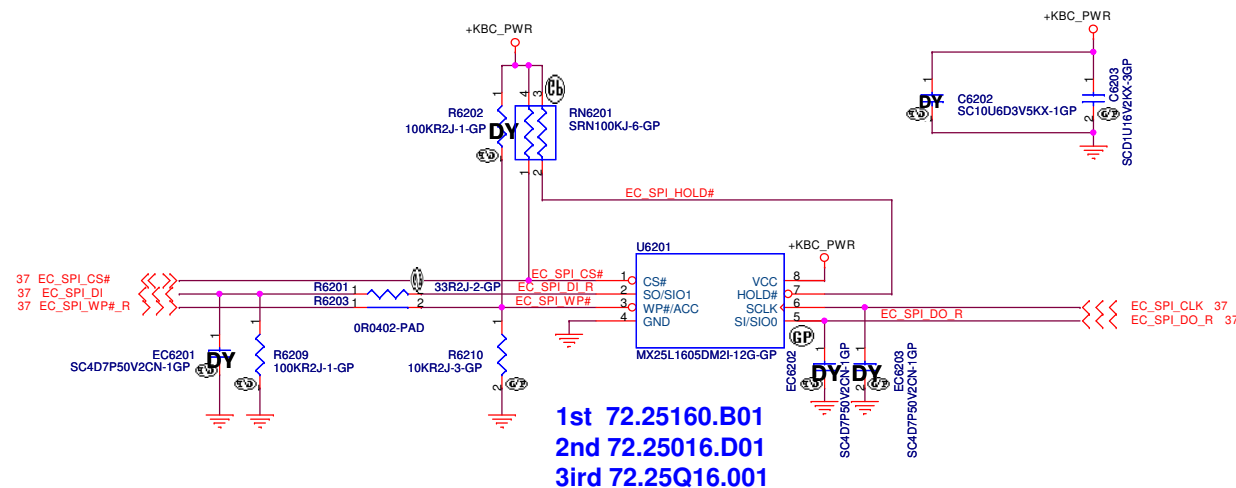
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

LAN differential signals use 100 Ohm impedance



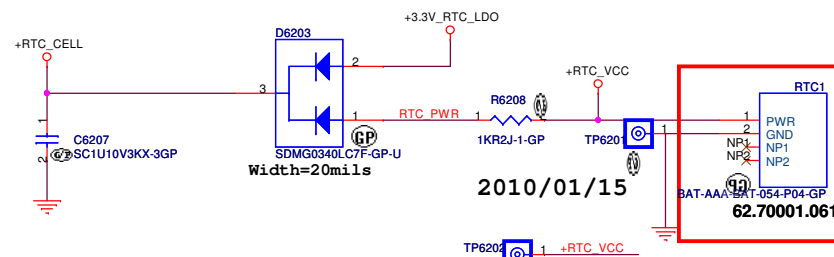
10/100 LAN surge circuit

SPI FLASH ROM (16M bits) for KBC



SSID = RBATT

RTC Connector



<Core Design>

DELL

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number

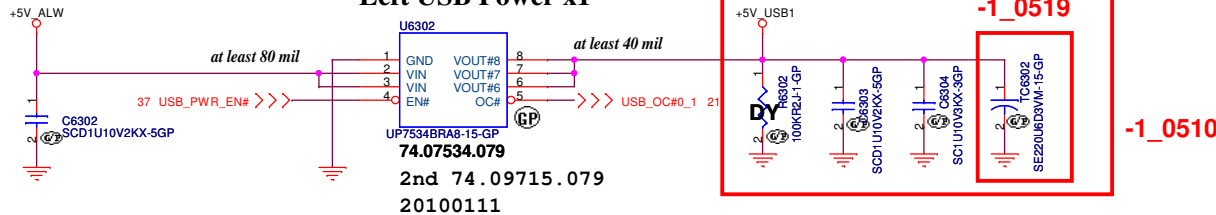
DJ2 Montevina UMA

Rev	YOC
-----	-----

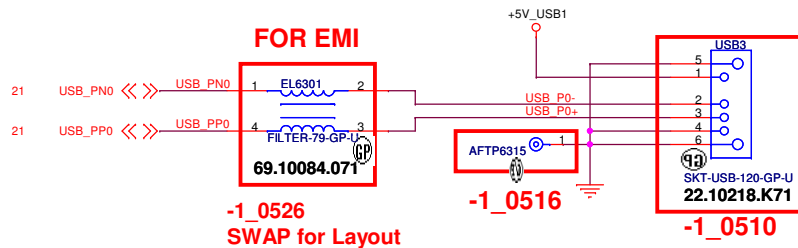
Date: Wednesday, June 02, 2010

Sheet 62 of 88

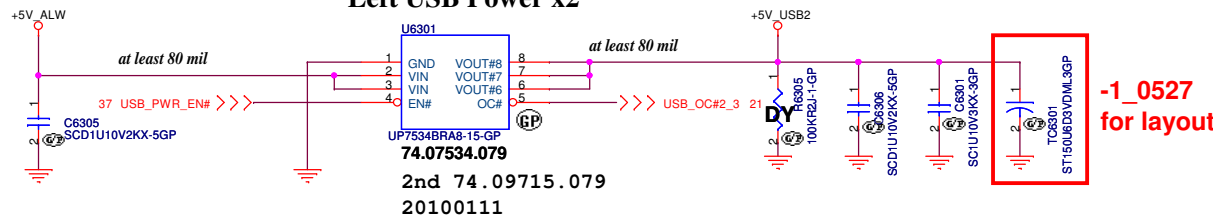
Left USB Power x1



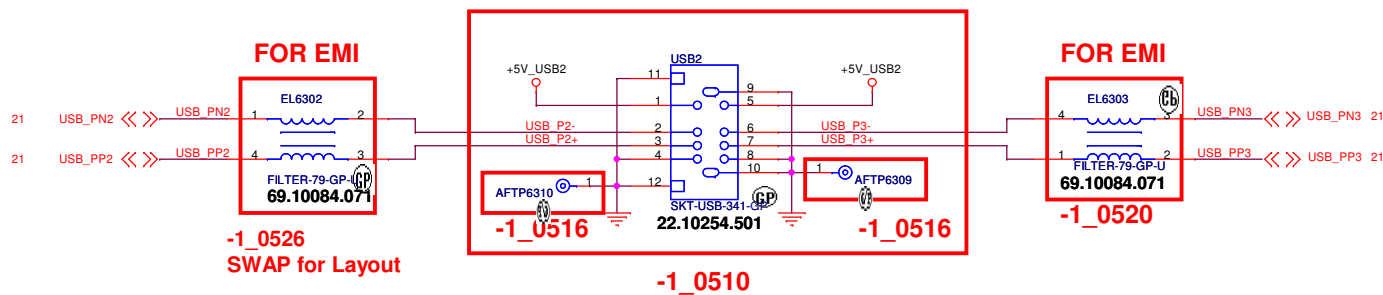
FOR EMI



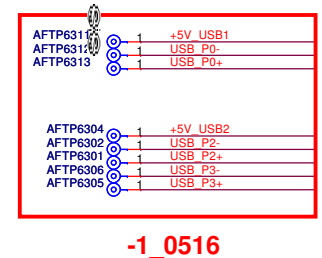
Left USB Power x2



FOR EMI



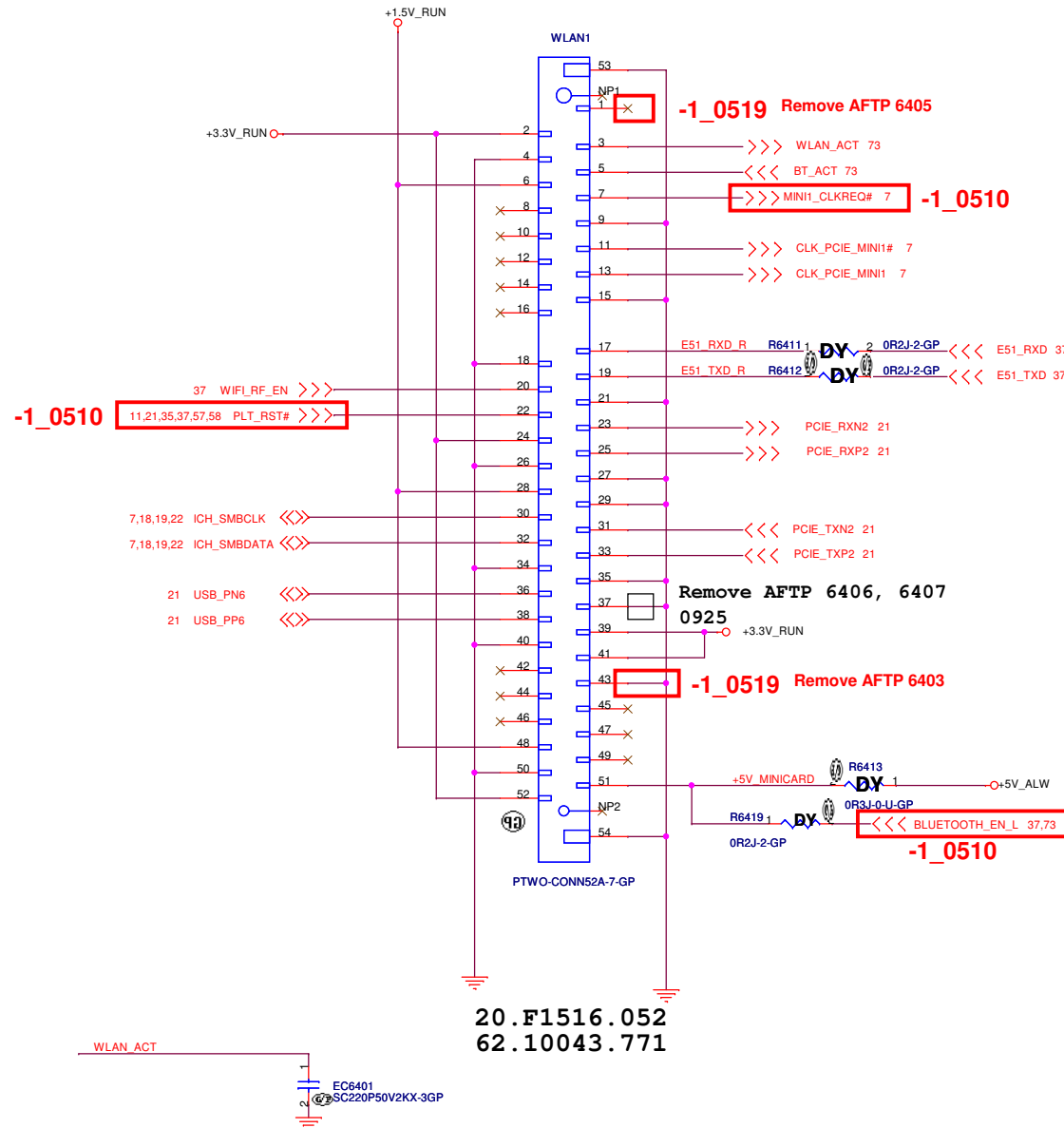
FOR EMI



<Core Design>

Mini Card Connector(802.11a/b/g)

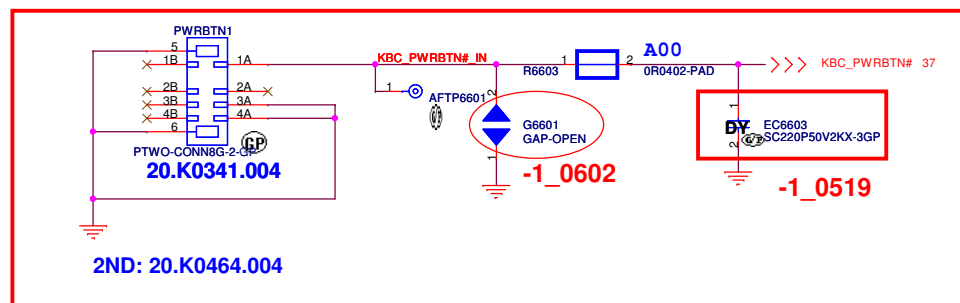
SSID = Wireless



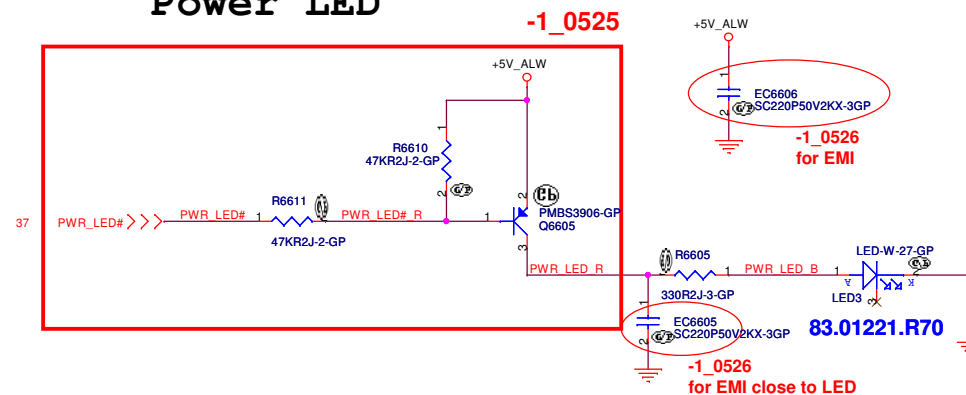
<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MINICARD			
Size	Document Number	Rev	
A3	DJ2 Montevina UMA	X00	
Date:	Wednesday, June 02, 2010	Sheet	64 of 88

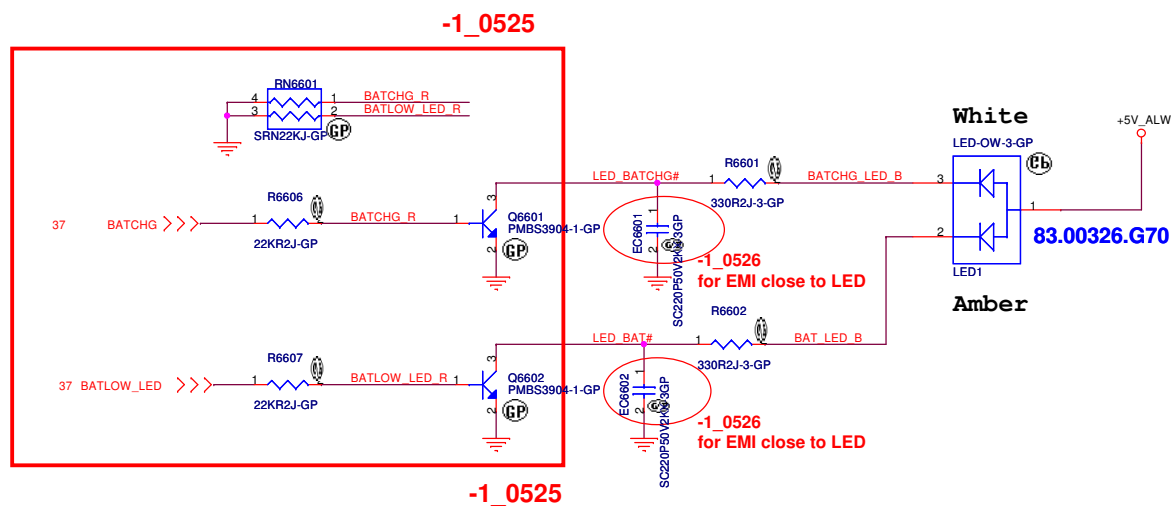
Power BTN Connector



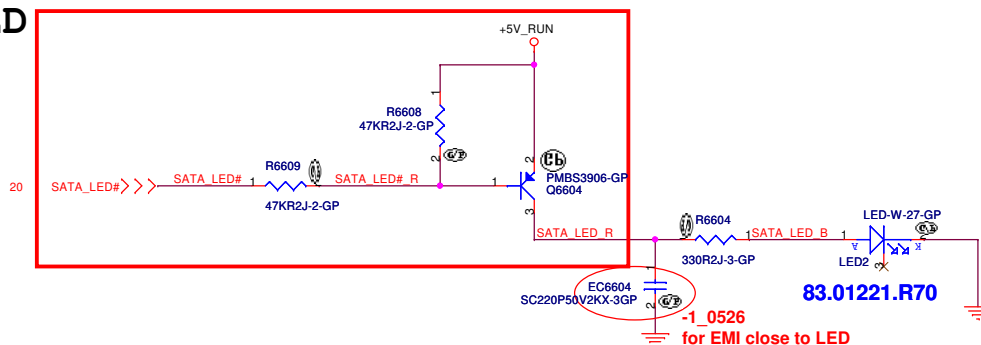
Power LED



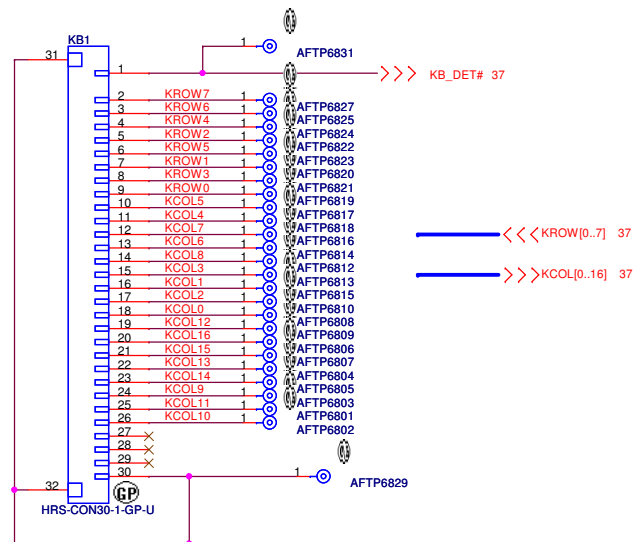
Battery LED



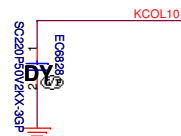
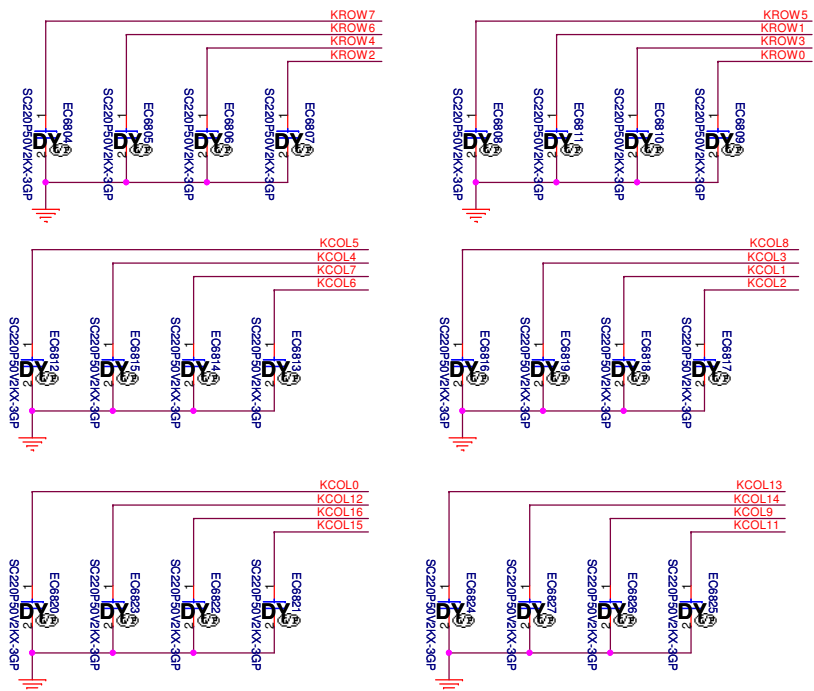
HDD LED



Internal KeyBoard Connector

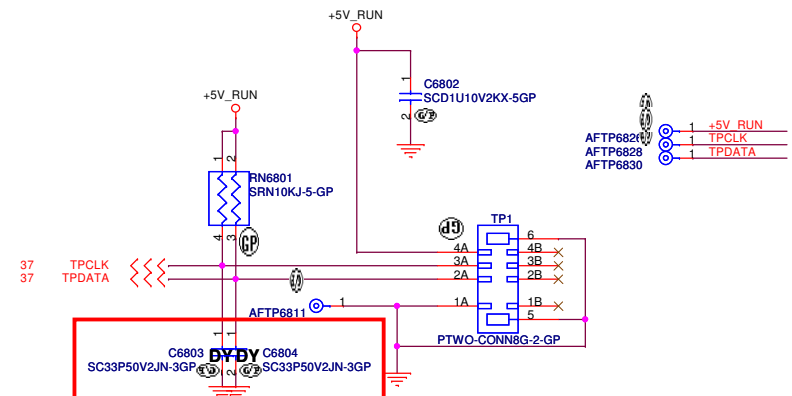


Main 20.K0421.030
20.K0259.030



```
SSID = Touch.Pad
```

TouchPad Connector



-1_0519

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size
A3

Document Number	
-----------------	--

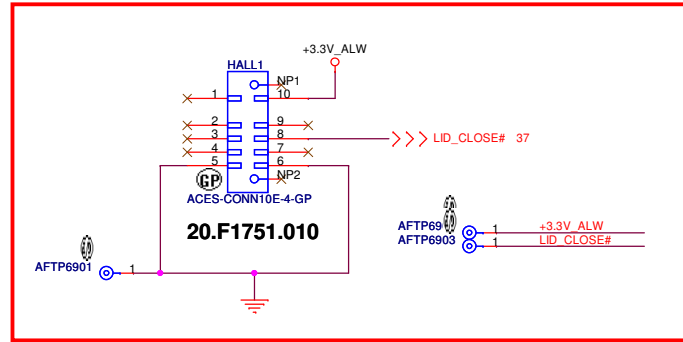
DJ2 Montevina UMA

Rev	X00
-----	------------

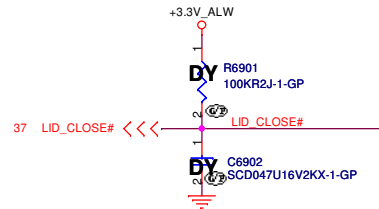
Date: Wednesday, June 02, 2010

Sheet 68 of 88

WWW.AliSaler.Com



-1_0511



-1_0516

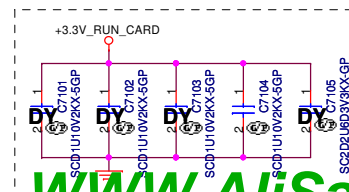
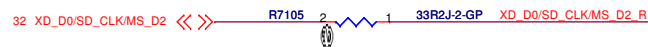
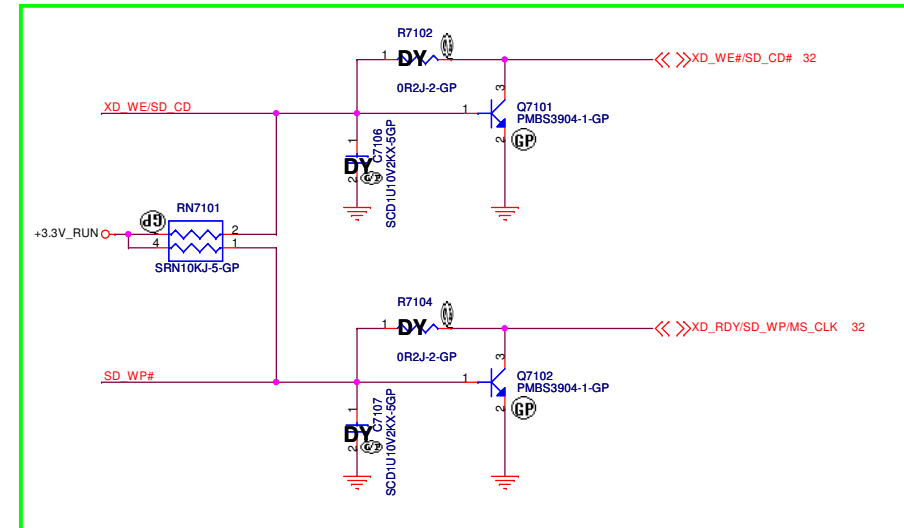
<Core Design>



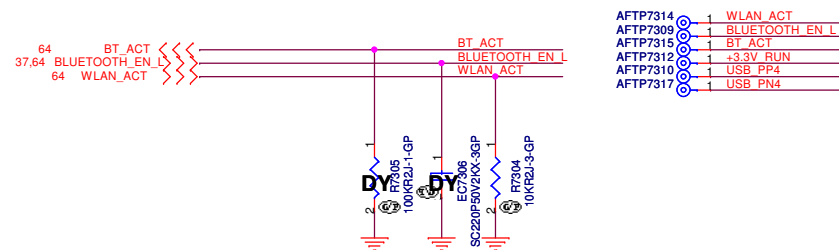
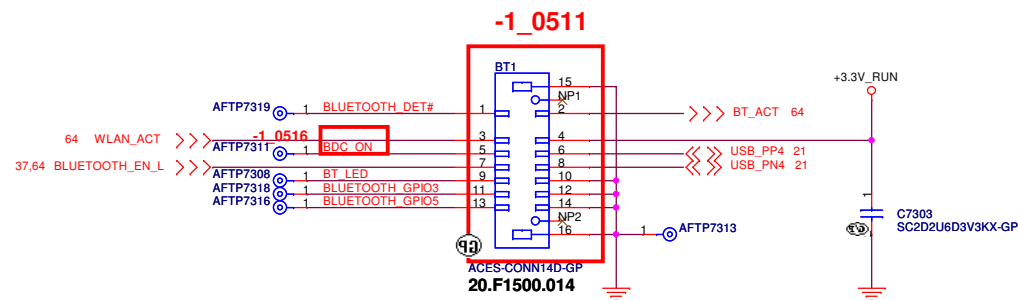
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Hall Sensor	
Size	Document Number			Rev
A3	DJ2 Montevina UMA			X00
Date:	Wednesday, June 02, 2010	Sheet	69	of 88

SD_WP#
No Card : LO
Inser Card : HI



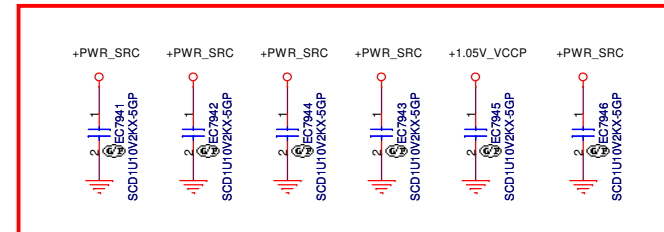
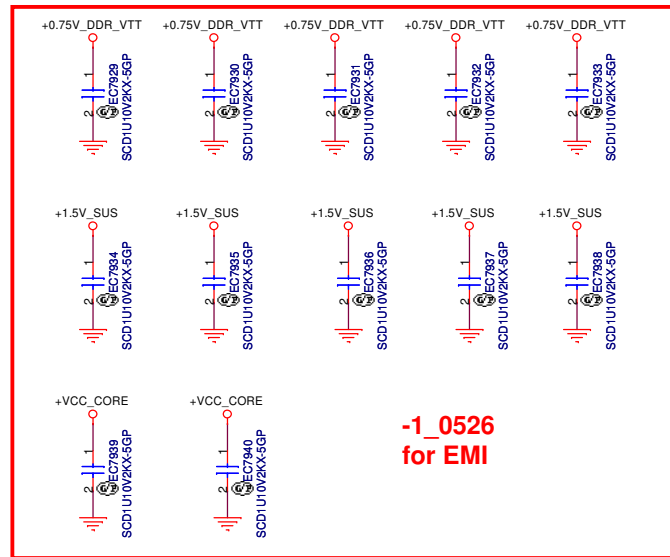
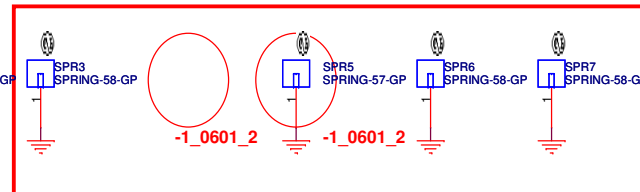
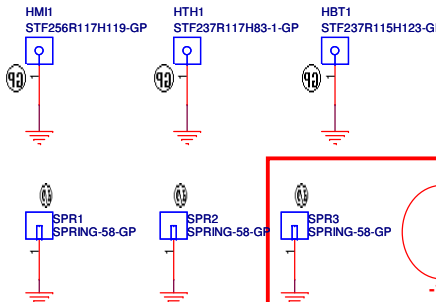
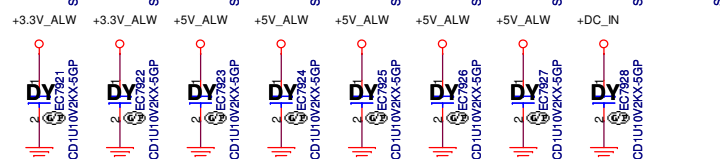
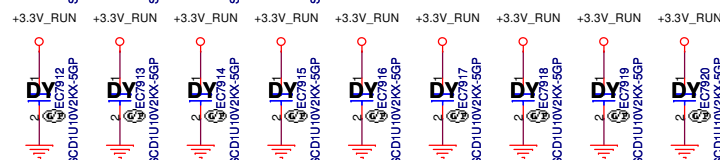
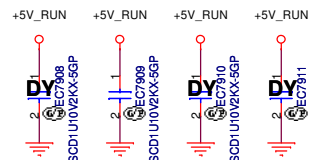
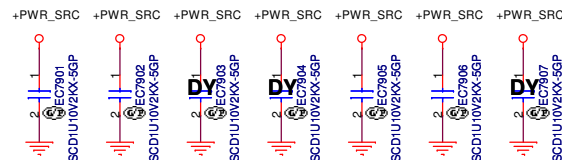
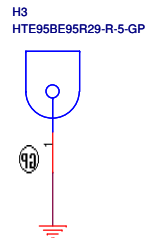
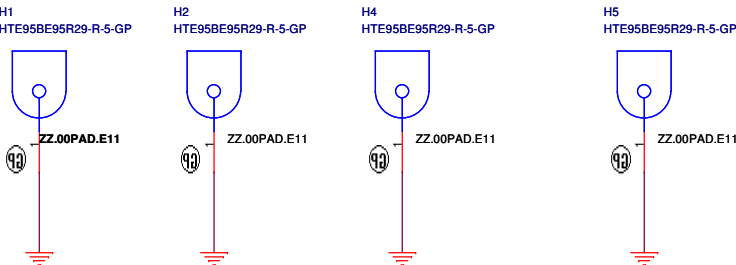
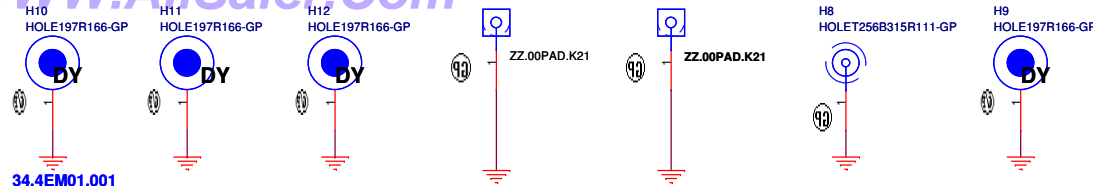
SSID = User.Interface



<Core Design>

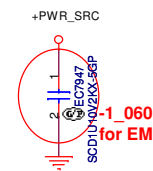
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Bluetooth	
Size	Document Number	Rev		
A3	DJ2 Montevina UMA	X00		
Date:	Wednesday, June 02, 2010	Sheet	73	of 88



-1_0528
for EMI

-1_0529
for EMI



-1_0526
for EMI

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		UNUSED PARTS/EMI Capacitors	
Size	Document Number	Rev	
A3	DJ2 Montevina UMA	X00	
Date:	Tuesday, June 01, 2010	Sheet	79 of 88